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No. 64

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CONTENTS

HARDWARE

Socialist Integration Responsible for Success in Memory Unit Production 1

Industrial and Scientific Cooperative Effort in Development . 6

Approximate Computation of Efficiency of Multibus Computer Systems 8

Small Multipurpose Peripheral for Microprocessor Systems 9

YeS-1060 Computer Awarded State Mark of Quality 12

Communications Organization Method in Multimicroprocessor System 13

SOFTWARE

Program Preparation System for Control Multimicroprocessor .. 15

System for Debugging Data Exchange Programs for Special-Purpose Computers 18

Interface for Graphic Representation of Programs in R-Technology 20

Structural Solutions and Methods of Organizing Computing Process in Muticonsole Graphic Complex 22

Software Package for Analysis and Synthesis of Uncontrolled Motion of Flying Vehicles (Principles of Design and Implementation) 23

APPLICATIONS

Computer Crime in Kirghiz SSR 26

YeS1010-Based Controller for Instrument Bus in IEC Standard . 27

Multifunctional Processor for Processing Seismic Prospecting Information 29

Designing Data Teleprocessing Systems in Automated Control Systems by Using MPD-3 and AP-1 33

ORGANIZATIONS

Institute of Cybernetics Wins Award 39

CONFERENCES

Microcomputers Control Production 40

PUBLICATIONS

Table of Contents From Journal 'CONTROL SYSTEMS AND MACHINES', November-December 1981 41

Microprocessors in Control and Communications 44

SOCIALIST INTEGRATION RESPONSIBLE FOR SUCCESS IN MEMORY UNIT PRODUCTION

Moscow EKONOMICHESKOYE SOTRUDNICHESTVO STRAN CHLENOV SEV in Russian No 8, Aug 82 pp 64-66

[Article by Georgi Varnov, chief director of Associated Plants of Memory Devices, Plovdiv]

[Text] Creation and development of our enterprise is a clear indicator of the advantages of socialist economic integration. A number of specialized plants for production of computer equipment was created in Bulgaria in the system of the State Economic Association IZOT after the agreement on cooperation in the field of development, production and use of computer equipment was signed in 1969 by the Peoples Republic of Bulgaria, the Hungarian Peoples Republic, the GDR, the Polish Peoples Republic, the USSR and the CSSR. The plant of memory units in Plovdiv was specialized in production of tape units and data preparation devices. It became the largest supplier of this product within a short time. The average annual growth rates were 59 percent during the period 1971-1975 and 16.5 percent during 1976-1980. It is planned to double the volume of production during the current five-year plan. The nomenclature of products of the plant is continuously being expanded and improved. During the past 12 years, 10 types of tape unit for large computers and 5 types for small computers, 7 types of magnetic tape data preparation devices, a number of instruments for debugging and repair and so on were assimilated.

Product improvement proceeded by increasing the speed of the carrier, the data recording density, dependability and operating reliability of articles. We demonstrated our success in this field at the exhibition at the Technical Center of GKhO [State Economic Association] of IZOT at Moscow, which was held from 26 through 30 October 1981. Various types of tape memory units with carrier speed from 0.32 to 5 m/s and recording density from 32 to 246 bit/mm, improved data preparation devices and service equipment for the CAMAC system for automation of scientific experiments were shown. Soviet specialists displayed great interest in the exhibition and gave high marks to our achievements in the field of improving memory units.

The continuously increasing demand for our product is the result not only of the high technical level of the articles but also of their operating dependability and reliability. The greater part of the plant products has been awarded the State Emblem of Quality. Introduction of a complex quality control system, developed and used at enterprises of L'vov (USSR), contributed to this. This system was directed toward increasing the responsibility of workers, specialists and managers for product quality.

The achievement of great success in production of the most complex articles within short deadlines became possible only under conditions of successful implementation of the general party line for the country's socialist industrialization on the basis of specialization and cooperation of production and accelerated development of science and technology. The labor of the collectives of a number of other enterprises of GKhO IZOT was included in the articles produced by our plant. More than 40 specialized enterprises deliver make-up articles to us.

Cooperation with science is a distinguishing feature of our development. New articles are developed at the Institute of Computer Equipment, GKhO, IZOT in Sofia. Individual design problems of articles and production technology must be solved in cooperation with the scientific institutes of industry, higher educational institutions and the Bulgarian Academy of Sciences.

The first steps in development and assimilation of production of memory units in the Peoples Republic of Bulgaria were made in close cooperation with Soviet scientific organizations and industrial enterprises. Production of the IZOT-5012M tape unit for the Minsk-32 computer was developed and organized. Production of this device over a number of years comprised the basis of our production program. Scientific and technical cooperation played an important role in accelerated assimilation of new generations of units for the YeS EVM [Unified Computer System] and data preparation devices.

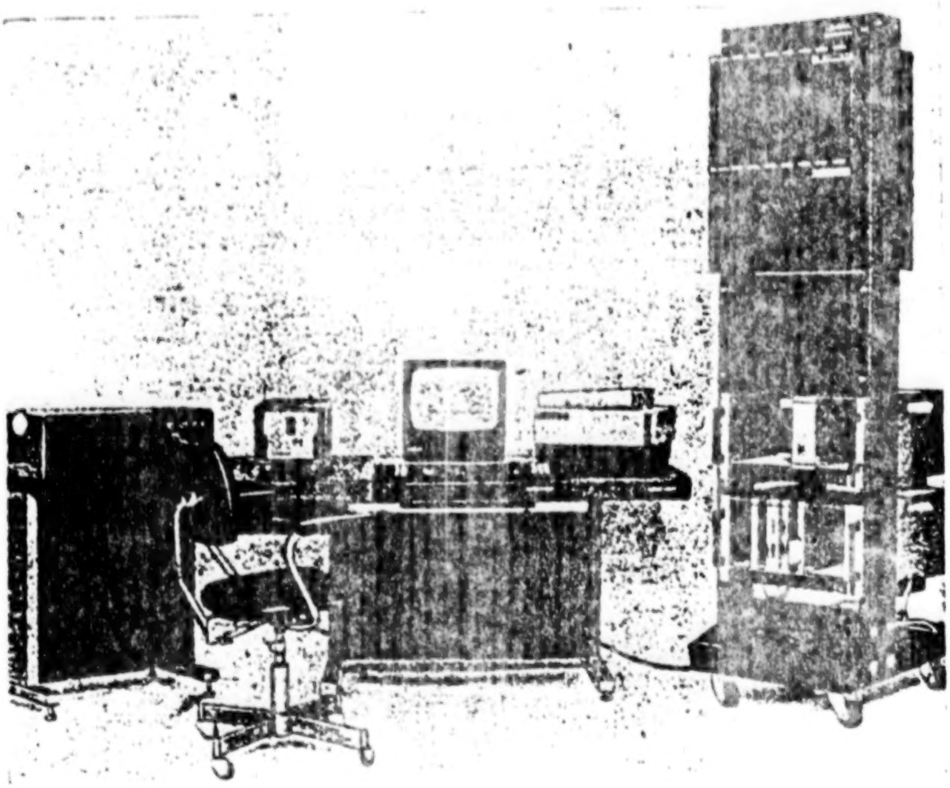
Our cooperation was implemented in the most diverse forms: coordination of plans for development of new articles, joint determination of technical parameters, exchange of specialists, joint testing of experimental models and so on. Personal comradeship and friendship were born and strengthened in the work of our and Soviet specialists and managers.

Scientific and technical cooperation with other socialist countries is being developed. Joint work with specialists of the GDR resulted in mass use of magnetic tapes produced by the ORWO Company. Problems of production, checking and use of tape units for small computers are being developed together with Hungarian specialists. During the past few years our vocational training center has trained more than 80 specialists and workers from the Hungarian Peoples Republic, the GDR, the Republic of Cuba, the USSR and CSSR in maintenance and repair of devices produced at the plant.

The export of our products to the fraternal socialist countries will increase continuously under conditions of mutually advantageous cooperation. It doubled during the period 1976-1980 compared to the level in the preceding 5-year plan. Approximately the same rate is also being maintained for the period 1981-1985. More than 10 plants in CEMA member countries that produce computer systems now receive our products. Moreover, scientific and technical progress in the field determines the continuous increase of the requirements of our customers on the technical parameters of produced devices, specifically on the

Assembly Department for Production of Tape Units

speed of data exchange and operating reliability and dependability. This forces us to increase the rates of scientific research and design work and to accelerate introduction of the results achieved into production. Thus, specialists of the Institute of Computer Equipment and of our plant developed and assimilated within one year production of the most complex device for use in the small computer system.



CAMAC System for Automation of Scientific Experiment

The decisions of the 12th BCP Congress posed new, more complex tasks to our collective in the field of technical progress. It was primarily necessary to raise production devices to a new technical level. New devices with higher technical parameters will be put into production each year. During the current 5-year plan, we should organize production of tape units which will be equal to the best worldwide models in main technical parameters. Further development of cooperation with scientific institutes and production associations of the USSR Ministry of the Radio Industry and Ministry of Instrument Building, Means of Automation and Control Systems contributes to successful fulfillment of these plans.

The high rates of development of production and assimilation of new, more complex devices determine the need for modernization, reconstruction and expansion of production funds. Developments of new organizational forms and changes of structure require new conditions; therefore, since 1 July 1980 the Plant of Memory Units was reorganized into the Associated Plants of Memory Units. It now includes a mechanical plant, plant of memory units, production equipment plant, electronic equipment plant and a specialized planning and design office.

The workers of our enterprises make an important contribution to the success achieved. The average age of the collective is approximately 30 years. More than 400 persons with higher education work in our collective and the majority of personnel has a secondary specialized education. All workers and salaried employees participate actively in the socialist competition for fulfillment of party decisions. Many of them have labor medals.

The collective of the Associated Plants of Memory Units is looking confidently toward the future. The basis of this confidence is the decisions of the 12th BCP Congress on acceleration of technical progress and further intensification and expansion of economic cooperation and of socialist integration.

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INDUSTRIAL AND SCIENTIFIC COOPERATIVE EFFORT IN DEVELOPMENT

Riga SOVETSKAYA LATVIYA in Russian 30 Apr 82 p 2

[Article by E. Yakubaytis, vice-president, Latvian SSSR Academy of Sciences, and V. Lysenkov, general director of the "Al'fa" Production Association, "Science to Production: Fruits of Joint Creativity"]

[Excerpts] The "Al'fa" Production Association and the Institute of Electronics and Computing Technology, Latvian SSR Academy of Sciences, are engaged in a joint effort to find forms of organization and planning of cooperation that will enable solving a broad range of scientific problems in compressed terms.

The institute and the association are cooperating in three areas: development of new semiconductor devices called integrated circuits, development of measuring equipment needed to support technological processes, and design of an information and computing network for the association.

The aim of the entire complex of efforts is to develop new methods that allow accelerating the operation, expanding the frequency range and simplifying the structure of processors that handle signals and implementing these processors in the form of integrated circuits.

This is all related to a large spectrum of research and to solving various problems in the theory of information and engineering cybernetics such as isolation and definition of useful signals in a background of noise and interference, classification of them, discovering hidden periodicities, investigating the parameters of distribution of wave and vibratory processes in various media, processing of speech signals and images to input them into computer networks, etc.

Especially topical and practically exceptionally important is the problem of developing new automated methods for monitoring the production of integrated circuits and using them as the basis for developing precision, highly productive equipment. The developed methods and algorithms for finding and analyzing defects have been incorporated into a specialized, high-speed image analyzer. This is the basic device for establishing visual, automated checking of integrated circuits.

The methods of visualizing information on a television screen have also been used in apparatus for checking semiconductor memories.

Thanks to modeling the physico-chemical processes occurring in integrated circuits, it has been possible to make a complex of apparatus designed for automatic checking of the characteristics and parameters of integrated circuits. Their dependence on temperature is analyzed, corrosion resistance is studied, and leaks of electric currents are determined.

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APPROXIMATE COMPUTATION OF EFFICIENCY OF MULTIBUS COMPUTER SYSTEMS

Kiev UPRAVLYAYUSHCHIYE SISTEMY I MASHINY in Russian No 6, Nov-Dec 81 (manuscript received 9 Dec 80, after revision 31 Mar 81) pp 45-49

[Article by Yuriy Mikhaylovich Sokol, engineer (Moscow)]

[Excerpts] Queueing theory is widely used to study complex systems. Markov models of queueing systems that model the operation of complex multiprocessor systems are described by a large number of states, which considerably increases the difficulties arising when these models are used. The practical need to study the functioning of complex systems has led to the development of approximate methods based on decomposition of the system into simpler components lending themselves to analytic study [4-7].

Discussed in this work is a multiprocessor computer system with several memory modules and several buses connecting the processors to memory; connected to each bus are several processors that are linked only to this bus and that share it in time among themselves. Given in this work is an approximate method for computing system efficiency based on breaking it up into single-bus systems; an estimate of the accuracy of this method is made.

Studying the throughput of multibus systems has shown that increasing the number of buses increases system throughput. Therefore, to raise overall system efficiency, multibus systems should be built with the pipeline structure and with the use of multiport memory modules [3]. The method elaborated in this work is an efficient tool for studying the efficiency of these systems.

This method of computation was used in assessing the throughput of multiprocessor systems designed on the base of the "Elektronika NTs-05" microcomputer now under development.

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SMALL MULTIPURPOSE PERIPHERAL FOR MICROPROCESSOR SYSTEMS

Kiev UPRAVLYAYUSHCHIYE SISTEMY I MASHINY in Russian No 6, Nov-Dec 81 (manuscript received 27 May 81) pp 137-138

[Article by Rostislav Yakovlevich Chernyak, candidate of engineering science, and Vladimir Pavlovich Rukhadze, engineer; both from the Institute of Cybernetics, UkSSR Academy of Sciences (Kiev)]

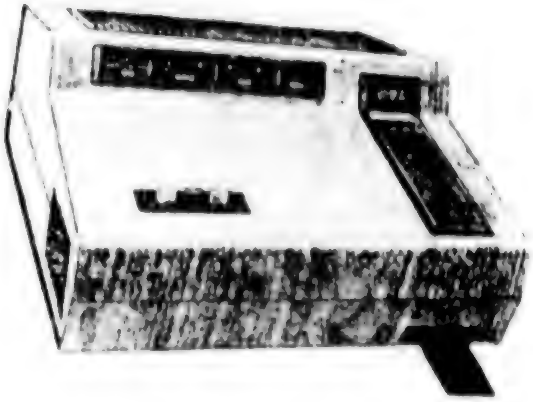
[Excerpts] The low level of operating characteristics of modern peripherals does not meet the requirements of rapidly evolving mini and micro computers and causes restrictions and difficulties in developing information processing systems based on them. The problem of developing peripherals for microprocessor systems is becoming ever more severe and urgent. In addition to the usual requirements such as high efficiency, reliability and others, imposed on the hardware for information acquisition, storage, preparation, input and output are the requirements of small size, compactness, convenience in accessing and good compatibility with mini and micro computers.

This article describes the small, relatively inexpensive peripheral for microprocessor systems that was developed at the Institute of Cybernetics of the UkSSR Academy of Sciences. It is mainly used as an input/output [IO] unit.

The following is a brief description of the multipurpose small device intended for recording, storing and reading information from magnetic media (see photo).

The device consists of the mechanism for moving a magnetic card in a circular channel with a unit of universal magnetic heads, slot for medium insertion and valve for output of the medium, reproduction amplifier unit, unit of drivers for record current and erase current, buffer storage unit and circuitry for interfacing the device to other devices.

The following modes are provided for recording information:
--start-stop (stepped) movement of the medium at the unit of magnetic heads when the data comes from transducers and devices with the asynchronous mode of outputting discrete information and a large data spacing period;
--continuous one-time movement of the medium at the unit of magnetic heads when the data comes from transducers and devices with the synchronous mode of outputting discrete information; and
--continuous cyclic movement of a card at the unit of magnetic heads when the data comes from both types of devices.



The following modes are provided for reading information:
--continuous one-time movement of the medium at the unit of magnetic heads when the data is output to high-speed synchronous receivers; and
--continuous cyclic movement of a card at the unit of magnetic heads to output data both to synchronous and asynchronous devices.

The availability of built-in buffer storage allows providing the quasi start-stop mode of device operation when writing and reading information.

During a write cycle, the contents of buffer storage are not erased; the data are kept for checking correctness of the writing by immediate reading after writing and bit-by-bit comparison with the data kept in storage. Using two-time reading of data with subsequent comparison allows a significant increase in the reliability of device information exchange.

Two versions of information storage are provided:
--on-line storage when the card is in the device circular channel and is moved continuously and cyclically at the unit of magnetic heads. Time for accessing an information file equal to card capacity is 250 ms;
--external or archival storage of cards filled on the device with basically unlimited volume of information.

At the user's option, the device can also copy data from one device to another, print out recorded data and output recorded data on a line display.

Specifications

Information medium	magnetic card 250 x 35 x 0.1 mm or section of magnetic tape 1000 x 35 x 0.075 mm
Type of medium	B-3914-35 or B-3806-35
Linear rate of medium movement	1 m/s
Capacity of magnetic card	1K bytes
Capacity of section of tape	4K bytes
Unit of magnetic heads	ten track with read/write heads
Medium durability	can be used at least 100,000 times
Buffer storage capacity	1K bytes

Power	220V ± 10 %, 50 Hz
Power consumed	30 W
Dimensions	290 x 230 x 135 mm
Weight	6 kg

The small, multipurpose device can be used successfully in various information processing systems both as a standalone unit and in a complex with other devices. Industrial production of this input/output unit for microcomputers and microprocessor systems is planned in the near future at an enterprise in the USSR Ministry of the Communications Equipment Industry. Broad functional capabilities, low cost and high reliability allow including it as part of mini and microprocessor systems, peripheral systems for information acquisition and storage, systems for preparing data for entry into computers and other automatic equipment, for example for program-controlled machine tools, automated work stations, etc.

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YeS-1060 COMPUTER AWARDED STATE MARK OF QUALITY

Moscow SOTSIALISTICHESKAYA INDUSTRIYA in Russian 17 Feb 82 p 2

[Article by V. Starchenko, Minsk: "Million Instructions Per Second"]

[Text] The State Mark of Quality was recently awarded to the "YeS-1060" computer made by the Minsk Production Association for Computer Equipment. Specialists noted the high engineering level, operating reliability and fine quality of manufacture of the country's largest computer.

The "Sixty" is equipped with a system of microdiagnostics. In event of a malfunction, it itself signals the operator and prompts him as to where to find the trouble. When you consider how many technical innovations have been applied in it and how large the storage it has is, it becomes obvious how important such a capability is for this computer which was designed to solve the most complex scientific and technical, economic, information-logic and other problems. Its performance is also high: over a million instructions per second.

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COMMUNICATIONS ORGANIZATION METHOD IN MULTIMICROPROCESSOR SYSTEM

Kiev MEKHANIZATSIYA I AVTOMATIZATSIYA UPRAVLENIYA in Russian No 2, Apr-Jun 82 (manuscript received 13 Jul 81) pp 51-54

[Article by R. Marshner and V. Mattes, engineers, and V. P. Tarasenko, candidate of engineering science]

[Excerpts] Described below is the method organizing communications in an MMPS [multimicroprocessor system] that uses MP [microprocessors] now widespread with a 1-byte data format and 64K-byte addressing capability. This method is based on using a common bus and allows combining up to 16 microprocessors into a system and expanding addressable storage to 1M bytes (20 address bits). The common bus also achieves circuit simplicity for the communication system and higher speed than traditional MMPS's with a common bus.

The MMPS consists of 16 structurally separate modules: 15 are single-type microcomputers and the 16th is the common bus control unit (UUOSh) integrated with the microcomputers. Since the allocation of tasks between modules can vary in the process of operation, this MMPS should be classed as a locally distributed symmetrical system with a parallel instruction and data stream [2]. Information is exchanged between modules in the system through the common bus (OSh).

The common bus enables asynchronous (with respect to information exchange requests) communication between modules and can operate in two modes: burst and multiplex. Only one link between microprocessors is possible at any one time.

Let us call the microprocessor that has generated an information exchange request the master, and the microprocessor selected for the communication, the slave. Let us call the time interval in which one byte is sent through the common bus (together with the service signals) in the multiplex mode and some data file in the burst mode the common bus cycle. The common bus control unit controls the common bus cycles; it performs the functions of starting the common bus cycles, monitoring execution of them, handling microprocessor errors, and some service functions. The common bus has 20 lines to send addresses: four high-order bits specify the address of the slave module while the 16 low-order bits specify the address of the storage cell in that module. When sending the INTERRUPT signal, the contents of the 16 low-order bits are ignored.

This system of information exchange organization in an MMPS is relatively simple and is characterized by a higher transfer rate and greater functional flexibility than traditional systems with a common bus. It also implements a number of the capabilities of the more complex communication systems such as UNIBUS, MULTIBUS, and HP-IB [4, 5]. The system has been implemented on the base of the 1880 microprocessor family. Tests of the MMPS have proven the communication organization method selected and the operating capability of the entire system. The MMPS can be used as a service system for a central processor in a large computer and as a microcomputer with expanded capabilities (multiprogram processing) for control.

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SOFTWARE

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PROGRAM PREPARATION SYSTEM FOR CONTROL MULTIMICROPROCESSOR

Kiev UPRAVLYAYUSHCHIYE SISTEMY I MASHINY in Russian No 6, Nov-Dec 81 (manuscript received 13 Feb 81) pp 68-69

[Article by Robert Israilevich Belitskiy, candidate of engineering science, Institute of Cybernetics, UkSSR Academy of Sciences (Kiev); and A. Ya. Boyko]

[Excerpt] The simulation system described below was developed to debug systems and applications software and to simulate control, general-purpose, multimicroprocessor systems with a one-channel common bus and distributed operating system. Also, the models of elementary processors and common memory that are part of the simulation system form the nucleus of the cross system intended for translating applications programs from parallel assembler to the microprocessor instruction language and the control structures corresponding to the programs.

The multimicroprocessor system to be simulated consists of a set of homogeneous (technologically and functionally) elementary processors connected to a single-channel common bus by means of a distributed arbitrator for the bus [1], a considerable amount of common memory and generalized input/output [IO] devices. An elementary processor, in turn, consists of a microprocessor, local memory with a module of the operating system and a number of hardware units to implement operations for synchronization of parallel processes, dynamic and static backup of processors, etc.

The extended assembler of the multimicroprocessor system includes the following special statements [3-6] that permit description of parallel processes: synchronization statements P (semaphore), V (semaphore), WAIT (Boolean variable), WAIT (real variable = arithmetic expression), LET (Boolean variable) and LET (real variable = arithmetic expression); delimiters of parallel and sequential branches PARBEGIN, PAREND, BEGIN and END; delimiters of parallel loops PARALLEL FOR and END; statement for restart of branch or parallel loop INTERRUPT; descriptors of common data and semaphores COMMON and SEMAFOR; and descriptors of branches and statements to be checked TEST and CHECK.

The system for simulating the multimicroprocessor system to be described is used to determine the following: number of requests for seizure of the common bus per unit of time and how long these requests stay in the queue; dimensions of intra-processor buffers for storing system interruptions; number of branches executed simultaneously; number of processors participating in synchronous modes and the number of iterations in loops corresponding to them; processor idle and operating time;

and the job run time. It also allows debugging of systems (in the microprocessor instruction language) and problem (in extended assembler) software.

The simulation system includes two models of the microprocessor system. In the first, the source parallel program placed in common memory is a set of branches related to each other, the program of each of which is a random set of microprocessor instructions and calls to the operating system with specified statistical properties. The structure of branch links may also be defined statistically. This model is useful in choosing a specific version of an operating system with a class of problems and in investigating various parameters of a multimicroprocessor system.

In the second model, the source parallel program is an actual applications program obtained from the user's program through cross-assembly. This model allows debugging and the most efficient assembly or restructuring of the source program with regard to the existing system configuration.

The simulation system includes the generator of parallel programs, the cross-assembler, the model of the field of processors, the model of the common bus with the arbiter, the model of common memory and the model of input/output devices. The parallel program generator effects the generation of sequential programs, linked in the manner specified, which are random sets of instructions with specified statistical parameters. Generally speaking, this generator must be generated anew each time the valid information on the class of problems to be solved is extended. However, the simulation system being described includes the two generator versions required most often: The first generates a program from loosely linked branches with common depth of nesting and varying number of nestings and length; the second generates a program from parallel loops with varying lengths of branches, numbers of iterations in loops and number of loops.

The cross-assembler is a two-pass translator that translates problem programs from extended assembler into the microprocessor instruction language and places translated programs in the model of common memory. Since the multimicroprocessor system in question is a control system and consequently designed to solve a small number of problems known in advance, control tables can be built prior to computation that reflect the structure of the corresponding parallel algorithms. Models of these tables are also built by the cross-assembler in the model of common memory. In addition to its own functions in the simulation system, the cross-assembler effects the generation of a perforated tape with control information from the models of debugged programs and control tables; the tape can be input into the system through one of the input devices for the multimicroprocessor system.

Simulated in the model of the field of processors are the file of elementary processors of variable length, execution of microprocessor instructions with regard to hardware expansions and the time responses of this execution (by using the file of counters of model time).

Simulated by the model of the common bus with an arbiter are the various disciplines of seizure of the common bus and transfer of information in the appropriate direction. Simulated in the common memory model are the cycle of memory seizure and read/write operations. Simulated by the IO device model are the operation and time responses of synchronous (exchange is forced by IN and OUT instructions) and asynchronous (exchange occurs according to readiness flags) devices.

This system for simulating multimicroprocessor systems has been implemented in PL/1 and YeS DOS Assembler. The size of the programs for the model for debugging the operating system (with the parallel program generator) is 110K bytes and that for debugging applications programs (with the cross-assembler) is 198K bytes.

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SYSTEM FOR DEBUGGING DATA EXCHANGE PROGRAMS FOR SPECIAL-PURPOSE COMPUTERS

Kiev UPRAVLYAYUSHCHIYE SISTEMY I MASHINY in Russian No 6, Nov-Dec 81 (manuscript received 13 Feb 81, after revision 23 Jun 81) pp 70-72

[Article by Sergey Kuz'mich Goncharuk, engineer; Vladimir Il'ich Pustovarov, candidate of engineering science; Vladimir Ivanovich Salapatov, junior scientific associate; and Aleksey Ivanovich Flerov, engineer; all from KPI [Kiev Polytechnic Institute] (Kiev)]

[Excerpts] The data exchange program debugging system is part of a system to automate programming of special-purpose microcomputers. This system was developed in the Department of Computer Science, Kiev Polytechnic Institute, by using the YeS OS macroassembler; it enables interpretation of programs for special-purpose microcomputers at the level of machine codes with adequate regard for time, including exchange instructions. It also enables simulation of information-time characteristics of the external environment at various levels of simulation and rapid restructuring of facilities for simulating external devices and the external environment when their characteristics and structure change. The compiler with the assembler and interpreter for the cross-system is adjusted to the required system of machine instructions for the special-purpose microcomputer by the method of macro generation; setting this up at present with consideration of corrections requires no more than a month from the time the final version of the specifications is approved.

Compared to other cross facilities for simulation, the system that has been developed allows a considerable reduction in labor input to describe objects of control and the external environment and elimination of the task of debugging simulation programs at the stage of simulating the real-time system being designed. The system affords the capability of natural extension of simulation programs for multimicroprocessor systems. The linguistic facilities in the simulation control language (elements of directives of second and third levels) and the language for descriptions of external objects and the external environment can be used in developing future systems to automate the design of control systems and complexes on the base of special-purpose microcomputers.

This exchange program debugging system has been implemented for two special-purpose microcomputers, the K580 IK80 microprocessor, and is in successful use. The system version with two levels for exchange program debugging allows simulating the operation of special-purpose microcomputers with up to 100K bytes of memory when the instrumental computer has 256K bytes of main storage.

Practical use of this simulation system has allowed a considerable reduction in capital, operating and time inputs in debugging a real-time system compared to the predictable inputs when the simulation modeling complex is used. Annual savings from system introduction is about 200,000 rubles. A version with three levels of debugging is now in experimental operation.

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INTERFACE FOR GRAPHIC REPRESENTATION OF PROGRAMS IN R-TECHNOLOGY

Kiev UPRAVLYAYUSHCHIYE SISTEMY I MASHINY in Russian No 6, Nov-Dec 81 (manuscript received 25 Aug 81) pp 73-78

[Article by Igor' Vyacheslavovich Vel'bitskiy, doctor of physicomathematical sciences, Institute of Cybernetics, UkSSR Academy of Sciences (Kiev); and Aleksandr Viktorovich Moshchitskiy, engineer (Vladimir)]

[Excerpts] A basic principle of R-technology is graphic representation of programs and data [1, 2]. However, before graphic input/output devices (primarily graphic displays and plotters) became widespread, it was believed that using the graphic form for writing R-programs and computers at all stages of graphic design and documentation of programs was not technologically efficient and not advisable. Therefore, the linear [3] and structurally linear [4] forms were created for writing R-programs, which adequately (by the simplest recodings made both that and the other way) corresponded to the graphic form of writing.

In R-technology in the stages of pre-machine design, the graphic form of writing was used; then the programmer switched to the linear form and entered it into the machine; then in the documentation stage, the linear form was automatically translated back into the graphic [5]. This technology, containing two translation stages from one form of writing (work, thought) to another, despite the closeness of these forms, naturally caused difficulties that reduced programmer labor productivity in R-technology.

The development and successful experimental operation in the YeS OS RTK [not further identified] of a translator from the graphic R-language to the R/TRAN language [6, 7] has now demonstrated the technological efficiency of switching to graphic representation of programs in R-technology for existing YeS7033 type alphanumeric printers. Used in these devices is the international standard height (2.2-2.3 mm) of the printed character and reduced spacing (3.17 mm) between lines on the printout listing. This has affected the esthetic makeup of the drawing of the R-program and has allowed using the standards of YeSSKD [Unified System of Design Documentation] for this purpose. No small role has also been played by the fact that graphic writing of the R-program is at least 20 to 30 percent shorter than linear writing in the R/TRAN language due to more efficient use of the printer list area.

In this article, we have formulated the principles of using graphic representation of programs in R-technology both for writing them in the R/TRAN language and for writing in the widely used FORTRAN and PL/1 languages that are included in the RTK as the basis for writing operations of the YeS OS RTK. Development of the unified technology for graphic representation of programs yields the capability of expanding and deepening fundamentally the existing technological methods, making the process of designing programs by R-technology even more efficient, and disseminating it for programming in widely used languages. Graphic representation of programs, unified at all stages of work, introduces into programming the concept of the drawing and the YeSSKD standards, proven by time, not only for hardware, but also for software.

The method of graphic representation of programs described in this article introduces into programming the concept of the drawing. This allows regulating and documenting the creative process of designing programs in accordance with the YeSSKD principles worked out over time, eliminating or substantially reducing the shortcomings of the traditional process of programming, and creating conditions for industrial preparation of programs by large collectives.

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STRUCTURAL SOLUTIONS AND METHODS OF ORGANIZING COMPUTING PROCESS IN MULTICONSOLE GRAPHIC COMPLEX

Kiev UPRAVLYAYUSHCHIYE SISTEMY I MASHINY in Russian No 6, Nov-Dec 81 (manuscript received 3 Apr 81) pp 81-85

[Article by Yefim Shulimovich Rayz, engineer, PO [Production Association] "Elektronmash" (Kiev)]

[Excerpt] The data base management system and monitor that have been developed are designed to enable interactive modes of operation of the POMGDK [problem-oriented multiconsole interactive graphic complex] based on the SM-4 control computer complex with the following graphic peripherals: from one to four graphic displays with buffer storage and special processor, and from one to four graphic information input devices and plotters. Real-time OS is used as the base operating system. The complex is intended for solving problems of interactive automated design, accumulation, conversion and editing of graphic information.

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SOFTWARE PACKAGE FOR ANALYSIS AND SYNTHESIS OF UNCONTROLLED MOTION OF FLYING VEHICLES (PRINCIPLES OF DESIGN AND IMPLEMENTATION)

Kiev UPRAVLYAYUSHCHIYE SISTEMY I MASHINY in Russian No 6, Nov-Dec 81 (manuscript received 8 Apr 81) pp 129-132

[Article by Vitaliy Mikhaylovich Belokonov, candidate of engineering science, Kuybyshev Aviation Institute, and Valeriy Dmitriyevich Yelenev, junior scientific associate, Kuybyshev Aviation Institute (Kuybyshev)]

[Excerpts] Software organization is now based on the systems approach in which software forms a unified system and not a set of autonomous programs for solving individual problems [1]. A result of this systems approach is the creation of software packages (PPP).

As a rule, software packages are oriented to solving problems from some applied field called the subject field of the package [2, 3].

The package for analysis and synthesis of the uncontrolled motion of flying vehicles (ANSIND) allows solving problems from this subject field.

It is evident that newly developed packages must take into account the specific nature of the computers on which they will be operated; in particular, this concerns selecting the operating system as the base for package development. The ANSIND package is intended for operation on small and medium Unified System computers and therefore in the YeS DOS environment (versions 2.1, 2.2).

The advantages of using YeS DOS instead of YeS OS on the computers of this class are given in [4].

The modern programming principle of modularity is the basis for the ANSIND package [5].

The capabilities of efficient implementation of modular programming on YeS computers stem from the object module obtained after translation from any language. Therefore, the ANSIND package is built in such a way that the modules forming the package are translated and stored in the object module library (BOM); this saves time because the source modules do not need translation for each run of a specific job using the package.

Structurally, the ANSIND package consists of the body which is a set of program modules, the organizing program-monitor and the package data base (BD) used to store results of computations and aerodynamics of specific flying vehicles (LA).

In developing the ANSIND package, much attention was paid to the process of optimal assembly of the package body which in the general case is reduced to development of a complex of noninterlaced program modules. In the case of nonoptimality of the package body, "...there is duplication of effort in the programming stage which entails additional cost and complicates the complex debugging of the modules" [6].

The personal library of absolute modules is used to store the phases that implement the package service programs and the phases of the program-monitor.

To facilitate user operation with the ANSIND package, a problem-oriented language (POYa) related to the package subject field is used which does not require extensive programming knowledge on the part of the user.

Package Composition. The ANSIND package body consists of four libraries: problem programs (BPP), models of motion (BMD), methods of optimization (BMO) and service programs (BSP).

The problem program library includes programs directly related to the package subject field. The main types of problems handled by using the ANSIND package are:
--flying vehicle motion analysis (check computation) (ANALYS);
--generation of selections of implementations from results of manifold modeling of flying vehicle motion (SELECT);
--construction of identification models of the dependency of output controllable characteristics on input parameters (IDENT);
--finding optimal design parameters (SYNTH);
--determining maximum tolerances (guaranteed and probable) on the spread of design parameters for flying vehicles (ADMIS); and
--determining the main probability characteristics of output random parameters--results of modeling flying vehicle motion (VEKhA) [PROBCHAR].

The motion model library includes programs that allow flying vehicle motion modeling with varying degrees of labor-intensiveness and error. Computations of flying vehicle motion parameters can be performed by simulation models [7, 8], by models using mean equations [9], and by regression parametric models.

The optimization method library includes programs that implement various algorithms for finding the minimum of the function of many variables. The efficiency of the methods in solving problems from the field of flying vehicle flight dynamics has benn taken into account in the selection of the methods.

The service program library includes programs that have not been included in the other libraries, but are needed for functioning of the components in these libraries.

All program components in the ANSIND package are written in FORTRAN-IV.

Conclusion. Experience of industrial operation of the ANSIND package has confirmed the correctness of the principles upon which its development was based and has allowed making the following conclusions:

The ANSIND package affords simplicity in user interaction with the package, which is achieved by using the problem-oriented language of the user.

The package allows the user to expand the package libraries within the bounds of the requirements imposed on these libraries.

Using the package data base frees the user from routine work on reprocessing information to use it in other programs.

Any program component in the ANSIND package and package data base files can be used together with modules that are not part of the package. In this case, the required user job can be added before the statement //EXEC LNKEDT to the job for working with the ANSIND package.

The principles underlying the ANSIND package development allow it to be used as part of a higher-order system, for example a system for computer-aided design of flying vehicles.

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COMPUTER CRIME IN KIRGHIZ SSR

Moscow SOTSIALISTICHESKAYA INDUSTRIYA in Russian 5 Feb 82 p 2

[TASS report from Frunze: "Computer Machinators"]

[Text] Elementary eyewash was engaged in by the managers of the Information and Computing Center, Ministry of the Food Industry, Kirghiz SSR, who violated financial discipline in operations with electronic equipemnt. The gross machinations of the ill-fated "operators-schemers" were uncovered by the people's inspectors.

Judging by reports, the computers at the center were used at maximum load. Bonuses were earned accordingly.

But the secret to this "efficiency," as revealed in the inspection, turned out to be simple: The center managers were doctoring the books and violating the established limits of accounts with the customers. Almost a thousand rubles were illegally exacted, for example, from the Chuyskiy Production Agroindustrial Association. Also involved were figureheads who were just listed as workers at the center.

According to the representation of the city committee of the people's inspectorate, the director of the information and computing center, A. Artyukhin, was removed from his job and fined as partial compensation for the damage done to the state. The other fanciers of "schemes" with computers were also punished.

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YeS1010-BASED CONTROLLER FOR INSTRUMENT BUS IN IEC STANDARD

Kiev UPRAVLYAYUSHCHIYE SISTEMY I MASHINY in Russian No 6, Nov-Dec 81 (manuscript received 19 Mar 81) pp 54-59

[Article by Anatoliy L'vovich Kurakin, engineer, Institute of Oceanology, USSR Academy of Sciences; Nikolay Vasil'yevich Popenko, senior scientific associate, Presidium of USSR Academy of Sciences; Viktor Nikolayevich Ryzhenkov, candidate of engineering science; and Leonid Semenovich Sitnikov, doctor of engineering science, Institute of Oceanology, USSR Academy of Sciences; all from Moscow]

[Excerpts] A basic principle in developing information-measuring systems (IIS) is the standardization of measuring, recording and control instruments based on a standard information bus. Methods of standardizing various instruments based on the standard IEC 625.1 (GOST 26003-80, former designations: HP-IB, IEEE-488--75) are discussed in [1]. Questions of introducing a standard instrument bus are evoking ever more increasing interest [2, 3]. A feature of the IEC standard that is especially valuable in automating scientific research is the lack of rigid requirements on designs. This considerably facilitates introducing the standard and allows using it not only in laboratory apparatus, but also in various on-board, sounding and other devices and complexes. Considering the prevalence of the IEC standard abroad and its intensive introduction into the nomenclature of domestic measuring and computing hardware, the advisability of developing instrument bus controllers based on the most used types of small computers should be recognized.

Described in this article is a controller based on the YeS1010 computer. This computer is produced in the VNR [Hungarian People's Republic] and is used widely in the CEMA countries, especially for operation under difficult conditions. It has a well-developed structure of hardware and software. Experience in successful operation of the YeS1010 computer, particularly on scientific research vessels, has now been gained. The controller built on the basis of the YeS1010 computer allows development of very flexible and universal information-measuring systems that most fully utilize the extensive capabilities embodied in the standard.

The task of implementing the controller reduces to designing the hardware and software interface of two buses--the computer input/output [IO] bus and the instrument bus (fig. 1) [not reproduced]. Connection to the computer IO bus (the so-called minibus) is made through the standard AMS board [apparatus for intercomputer communications] (YeR-19 or interface for direct memory access) which organizes interaction with the central processor.

The efficiency of designing information networks based on the instrument bus is problematic; however, in this case, it is just a question of an additional capability of intermachine exchange playing an auxiliary role, for example, for emulation, emergency replacement of the computer, etc. Since controller units are already available in many types of computers in use (HP-2100, HP-9830, "Elektronika-60," UVK M400, RS-4401 and others), organizing data exchange with them over an instrument bus requires no additional physical inputs (for example, on the basis of the MIBIO [Microprogrammed Interface-Bus Input/Output] module described above).

In the process of practical application of the instrument bus, controller functions implemented by software are being developed further.

Implementing the controller for the instrument bus based on the YeS1010 computer expands the capabilities of introducing the IEC 625.1 standard. At the same time, the instrument bus is also a system facility for expanding the YeS1010 configuration along with the "mini" systems in use, the system known as a "real-time unit" and the CAMAC system.

The controller IK [interface card] that includes the interface assemblies is made as a YeS1010 interface card. Thus, the controller unit consisting of two standard interface cards joined by cable is installed in the computer chassis together with standard cards for interfacing external devices. The controller interface card circuitry is implemented with 66 packages of series 155 integrated circuits.

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MULTIFUNCTIONAL PROCESSOR FOR PROCESSING SEISMIC PROSPECTING INFORMATION

Kiev MEKHANIZATSIYA I AVTOMATIZATSIYA UPRAVLENIYA in Russian No 2, Apr-Jun 82 (manuscript received 26 Aug 81) pp 49-51

[Article by K. G. Samofalov, corresponding member of the UkSSR Academy of Sciences, V. A. Dyadyura and Yu. S. Kanevskiy, candidates of engineering sciences, and Yu. M. Zorin, V. V. Balyuk, V. I. Lozinskiy and A. V. Penenko, engineers]

[Text] Seismic information processing is characterized by manifold repetition of several single-type computational procedures. Analysis of programs used most often shows that almost all machine time is expended on executing 10-15 computational procedures. To raise productivity in seismic data processing, central processor [CPU] capacity has to be increased. This requires considerable increase in cost of equipment and complexity of operation. Another way is to develop special-purpose computing units that are connected to the computer and execute the operations most often encountered.*

To process seismic data, the Kiev Polytechnic Institute and the "Ukrgeofizika" PO [Ukrainian Geophysical Production Association] jointly developed a special processor that features higher throughput, considerable main storage and broad functional capabilities. The processor is a standard peripheral (VU) connectable to a computer communications channel. It has a standard interface that permits connection to a broad class of machines (for example, to all Unified System computer models and the latest ASVT [modular hardware system] models) without substantial changes to the computer software. Availability of internal storage in the processor allows organizing simultaneous fetching (with memory interleaving) which raises speed considerably.

The processor executes the following basic algorithms: convolution of route with operator, computation of cross-correlation function, addition of two arrays, multiplication of array by a constant, multiplication of two arrays, determination of slip mean array, and centering of array.

The processor has five main elements (see figure): channel interface unit (BSK) that supports data transfer, arithmetic unit (AU), main storage (OZU), control unit (UU) and index arithmetic unit (IAU).

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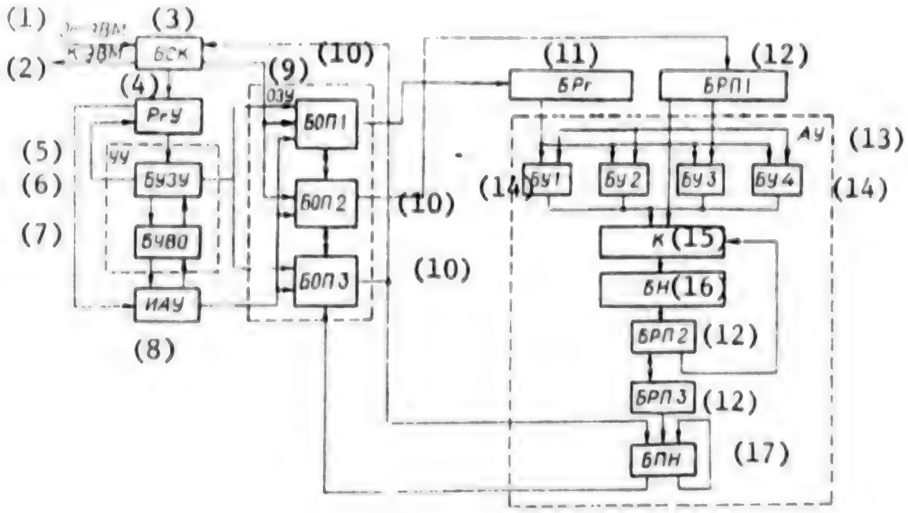
* V. V. Balyuk, V. A. Dyadyura, Yu. M. Zorin et al., "Speeding Up Seismic Data Processing by Special Processors of Varying Architecture," GEOFIZICHESKIY ZHURNAL, No 2, 1980, pp 39-45.

The channel interface unit (BSK) enables special processor communication with the computer selector channel, converts information formats, decodes channel commands, indexes and transfers status of the process and qualified status.

The arithmetic unit has a mainline structure that allows achieving maximum loading of the equipment when executing the most laborious algorithms (convolution, correlation types). There may be one, two or four multipliers (BU) in the arithmetic unit to enhance reliability.



Simplified Structural Diagram of Processor

Key:

1. from computer
2. to computer
3. BSK [channel interface unit]
4. RgU [control register]
5. UU [control unit]
6. BUZU [storage control unit]
7. BUVO [operation execution control unit]
8. IAU [index arithmetic unit]
9. OZU [main storage]
10. BOP1, 2, 3 [main storage unit 1, 2, 3]
11. BRg [buffer register]
12. BRP1, 2, 3 [register storage unit 1, 2, 3]
13. AU [arithmetic unit]
14. BU1, 2, 3, 4 [multiplier 1, 2, 3, 4]
15. K
16. BN [accumulator]
17. BPN [subadder and normalizer]

The multiplier is designed to multiply two 16-bit numbers to produce a full 32-bit product. A multiplication operation is executed in 1 μs. The accumulator (BN) is designed to add the products coming from the multipliers and allows parallel accumulation of four points of the result (with convolution and correlation type operations). The subadder and normalizer (BPN) is designed to execute the operation of subadding of results and multiplying the results of the current operation by the normalizing factor 2^{-S} and to detect overflows and output the appropriate service signals.

Main storage (OZU) performs the functions of storing the initial data and the intermediate and final results of the computations. It consists of the three units of main storage with random access (BOP1-BOP3). This storage design allows reducing the effective storage access cycle through simultaneous reading of two pairs of operands and writing of computation results in the third module.

The control unit (UU) includes two functionally separate units: operation execution control unit (BUVO) and storage control unit (BUZU). The operation execution control unit is designed on the microprogram principle in which a number of basic algorithms are kept in read-only memory [ROM]. There is also the capability of moving microprograms from computer memory to the microprogram ROM, which subtantially expands the functional capabilities of the special processor. A microinstruction 32-bit word contains 11 fields that enable execution of 80 instructions by the special processor. The storage control unit is designed to control exchange operations between main storage and other computer devices and units. It has fixed logic to generate control signals.

The index arithemtic unit (IAU) generates codes of addresses for access to main storage.

Register storage unit BRP1 executes the functions of distributing information that comes from main storage modules. Register storage units BRP2 and BRP3 are designed to store the intermediate and final computational results in the accumulator and subadder-normalizer. Each unit has four registers.

Execution of any algorithm is divided into three stages: input of source information into the processor, computation, and input of computational results into computer memory.

Coming in through the channel interface unit in the first stage are the computational algorithm code (if the microprogram for computations by this algorithm is not in the ROM, then the microprogram itself is sent from the computer to the microprogram control unit), the initial information arrays, each of which is written into its own main storage module, and the service tags. After the exchange with the selector channel is completed, the channel interface unit initiates the start of the computation.

As an example, let us consider the organization of processor functioning in executing the algorithm for convolution of the route with the operator.

The computation is performed according to this formula:

$$z_i = 2^{-s} \sum_{j=1}^{M} x_{i+j-1}\, y_j,\ i = 1, 2, \ldots, n,\ j = 1, 2, \ldots, M.$$

The algorithm for computation of the convolution permits natural paralleling of the computing process, in which several points of the result are computed simultaneously. Two pairs of operands x_{i-1}, x_i and y_{j-1}, y_j are read in each access to memory from the modules with random access. In each computation cycle, one of the operands x_1 is sent by parallel code to all the multipliers, while the other, y_k, goes to the first multiplier and is serially transferred from one multiplier to the next. The products computed in the multipliers are accumulated in the adder-accumulator.

Simultaneously accumulated in the adder are four points of the result, for the computation of which N + 3 cycles of multiplier operation are required.

Then, when the subadding flag is present, register storage unit BRP2 is connected to the subadder-normalizer where processing of the four accumulated points continues. At the same time, the next four points are accumulated in register storage unit BRP3, which is connected to the accumulator, etc.

The availability of a channel for exchange between the result memory module and initial data modules allows execution of a chain of algorithms without accessing the computer (or at least the number of accesses is reduced to the minimum).

The information to be processed is represented by binary numbers with fixed point in the 16-bit format in two's complement code.

Specifications

Rate of execution of operations with one-time execution and storage of statements in main memory, in thousands of operations per second:	
addition	700
multiplication	450
Same as above when working with arrays, in millions of operations per second:	
addition	4
multiplication	4
paired operation multiplication + addition	4
Control organization principle	microprogram
Microinstruction unit capacity	up to 1024 32-bit words
Instruction fetch cycle	90 ns
Main storage capacity	32K
Main storage access cycle	500 ns

There are 80 instructions in the repertoire.

The special processor is made with series 155, 131, 556 and 565 IMS [integrated microcircuits]. A prototype is currently being produced by the "Ukrgeofizika" Production Association.

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DESIGNING DATA TELEPROCESSING SYSTEMS IN AUTOMATED CONTROL SYSTEMS BY USING MPD-3 AND AP-1

Kiev UPRAVLYAYUSHCHIYE SISTEMY I MASHINY in Russian No 6, Nov-Dec 81 (manuscript received 17 Jun 80, after revision 26 Aug 80) pp 22-25

[Article by Vladimir Sergeyevich Bespalov, engineer, NPO [Scientific Production Association] "Lenelektronmash" (Leningrad); Yevgeniy Borisovich Butnikov, director PKTB [Planning and Design Technological Bureau] ASU [Automated Control Systems] "Rosmyasomolproma" (Ivanovo); and Genrikh Mikhaylovich Strizhkov, k. t. n. [candidate of engineering science], IIMF [Odessa Institute of Maritime Fleet Engineers] (Odessa)]

[Text] A major problem in expeditious production control is the task of timely presentation of information on the object of control to managerial personnel. This task can be implemented in modern automated control systems by using the methods and facilities of data teleprocessing. Meant by teleprocessing is the processing of data arriving from remote objects of automation , and the control of the transfer of this data through communication channels between them and a computer. Such forms of interaction are possible when subscribers are connected to a computer by using the appropriate set of teleprocessing hardware.

Discussed in this article is the experience of interfacing and operating the AP-1 (YeS8501) terminals of the YeSTEL complex with the MPD-3 (YeS8403) data communication multiplexer.

The need for studying interfacing of AP-1 terminals and the MPD-3 multiplexer is due to the need of meeting the ever increasing demand of control systems for data teleprocessing facilities.

Features of the AP-1 and MPD-3. Within the Unified System of Computers, there are hardware and software enabling a computer to process information and exchange it over communication lines with remote sources and consumers. Information can be exchanged over switched and unswitched communication channels.

The MPD-3 multiplexer is designed for exchange of information between remote subscribers and Unified System computers over telephone lines; it enables operation in the half-duplex mode for receiving and sending information. The MPD-3 can be connected to the multiplexer or selector channel on the computer; it enables connecting up to four telephone lines to a computer.

The AP-1 terminal is a complex of input/output [IO] hardware that enables data preparation and sending data to a communication channel, receiving information from communication channels, performing accounting and copying data from one medium to another. A structural diagram for a data teleprocessing system based on the MPD-3 and AP-1 is shown in fig. 1.

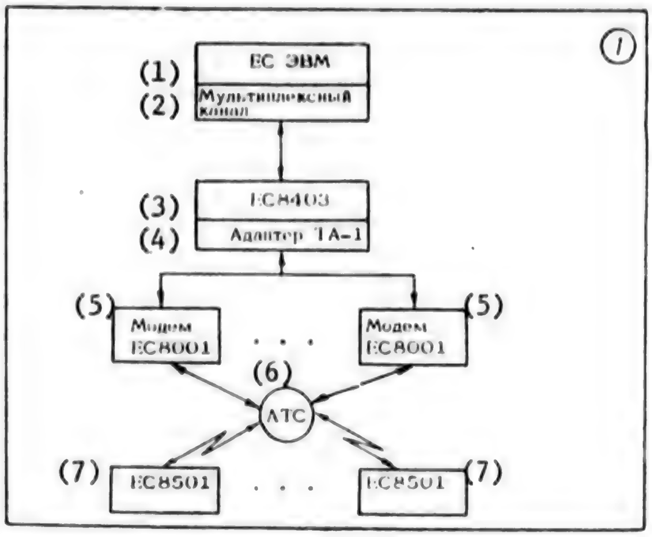

Fig. 1.

Key:

1. Unified System computer
2. multiplexer channel
3. YeS8403 multiplexer
4. TA-1 adapter
5. YeS8001 modem
6. ATS [automatic telephone exchange]
7. YeS8501 terminal

AP-1 - MPD-3 Interface Measures. Additional connectors have to be installed on the YeS8001 modem for compatible operation with the MPD-3. These connectors allow connecting the modem to the TA-1 adapter for the MPD-3 by the cables included with the adapter. The additional connectors are connected in parallel to connectors 02RV and 03RV on the modem. Connections and designations for the connectors are given in tables 1 and 2.

Table 1. 03RV (AVU [automated calling unit]) Pin Assignment

Circuit	Circuit Name	Pin	Connection
201	Signal ground	01	04-2
202	Transmit request	02	01-4
203	Data line busy	03	01-5
204	Remote station connected	04	01-6
205	Cease call	05	03-3
206	Digital signal 2	06	03-4
207	Digital signal 2	07	03-5
208	Digital signal 2	08	03-6
209	Digital signal 2	09	04-1
210	Request of next digit	10	04-3
211	Digit is being supplied	11	05-3
212	Protective ground	12	06-1 06-2
213	Power supply indicator	13	06-3

Table 2. 02RV (modem) Pin Assignment

Circuit	Circuit Name	Pin	Connection
101	Protective ground	01	09-1 09-2
102	Signal ground	07	05-1
104	Reception of data	03	06-1
105	Transmit request	04	06-2
106	Ready to send	05	06-3
107	Data transmission equipment ready	06	08-1
109	Detector of received line signal	08	08-3
103	Transmission of data	02	05-2
108.1	Connection of data transmission equipment to line	20	08-2
125	Call indicator	22	04-3

To provide for operation of the MPD-3 with the AP-1, switching in the TEZ [standard exchange cards] in the terminal has to be performed in accordance with table 3. When operating with dedicated telephone channels of communication, switching in the standard exchange cards in the YeS8001 modem has to be performed in accordance with table 4. When operating with switched telephone channels of communication, additional switching in accordance with table 5 has to be performed in addition to the switches specified in table 4. It is necessary to provide for a jumper between the connectors of the modem 02RV (pin 11) and 03RV (pin 12).

Use of Software. Compatible operation of the AP-1 with the MPD-3 and Unified System computers on the logical level can be afforded by development of software by using the Basic Telecommunications Access Method (BTAM) that is part of YeS DOS, versions 2.0 and 2.1.

The supervisor supporting the teleprocessing mode is used to develop programs in the operating package.

To confirm what has been stated above, operation of a Unified System computer with the MPD-3 and AP-1 over switched telephone lines was checked in the basic modes:
--subordination--with centralized control from the computer (operation CONTROL OF STATUS OF STATION);
--competition with the computer (operation POINT-POINT).

In developing programs for testing, we used the logical module BTAM that provides:
--logic for operation with buffers;
--elimination of errors together with the logic for counting errors for start-stop devices and local displays;
--logic for on-line testing of terminals;
--servicing of switched channels of communication;
--logic for recoding implemented in the macro instruction TRANSLATE;
--logic for servicing of telegraph apparatus; and
--logic for stopping of polling.

Table 3. AP-1 (YeS8501) Card Switches

	Terminal Number		
Card Number	Jumper Connected	Jumper Removed	Function Performed
0352	1-2		Inhibit response in direction of remote terminal
	06-07		Operation in competition mode
	15-16		Switch on circuit 108 with switch on of switch LIN
		19-20	Inhibit return current to line
		21-23	Switch on/off circuit 105 as a function of mode
		24-25	Operation with modem 200 bits/sec
0358		3-4	
		5-6	Response to general and group address
0359	1-2		Response is assigned (AK), during operation with block checks
	04-05		
	06-07		Block recognition method is specified
0360	1-2		Answering interval from receiving terminal is 2.5 s
0362		1-2	Operation in synchronous mode
	3-4		Transmission of characters with one "stop" bit
0365	01-02		Pause or no-pause is specified after transmission over the line of characters LF, LR, HT during operation between two terminals (TRM -- MPD in position TRM)
	04-05		
0368		01-02	When an error is detected, perforator automatically stops, backs up one position, cancels error, punches code and continues operation
0378	01-02		When the perforator has no verification sensors
0385	1-5		By code DS1, typewriter operation is authorized
	2-6		By code DS2, perforator operation is authorized
	3-7		By code DS3, typewriter is blocked
	4-8		By code DS4, perforator is blocked
0387	1-5		Rate of echange of information over the line is set
0367	01-09		Capability is determined of controlling operation of typewriter, perforator and reader by codes DS1-DS4, engaged over the line in remote control
	01-06		
	02-07		
	03-08		
	04-05		

Table 4. YeS8001 Modem Card Switches

Card Number	Terminal Number Jumper Connected	 Jumper Removed	Function Performed
008	22-23		Transmitter operation does not depend on status of circuit 105
0003	2-4		Sensitivity is lowered by 6 dB
0004	1-2-4		Selection is made of channel of potential circuit 126
009		1-2 3-4	When call signal is received, duration of readiness is set at 17 ± 2 s
	5-6		For operation with automatic call unit

Table 5. YeS8001 Modem Card Configurations

Card Number	Terminal Number Jumper Connected	 Jumper Removed	Function Performed
0008	1-3 1-4		Switches on generator of response type with F=2,100 Hz
	15-16		Ensures level of signal for autoresponse with F = 2,100 Hz
	19-20		Switches on circuit 106 with delay relative to circuit 105
	22-23		Operation of transmitter is independent of status of circuit 105
0009		1-2 3-4	Duration of readiness 17 ± 2 s
	5-6		Operation of modem with automatic call unit
0022	44-45		Operation of modem with automatic call unit

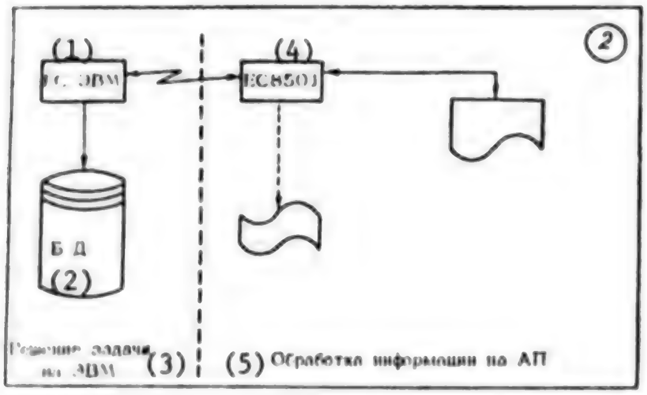

Fig. 2

Key:
1. Unified System computer
2. Data Base
3. Computer job run
4. YeS8501
5. Information processing on terminal

Key:
1. shops
2. department of production planning
3. plan
4. YeS8501 terminal
5. listing of transfer
6. preparation of entry information and input of it into computer
7. YeS1022
8. data base
9. computer job run
10. YeS8501
11. Processing of output information on terminal

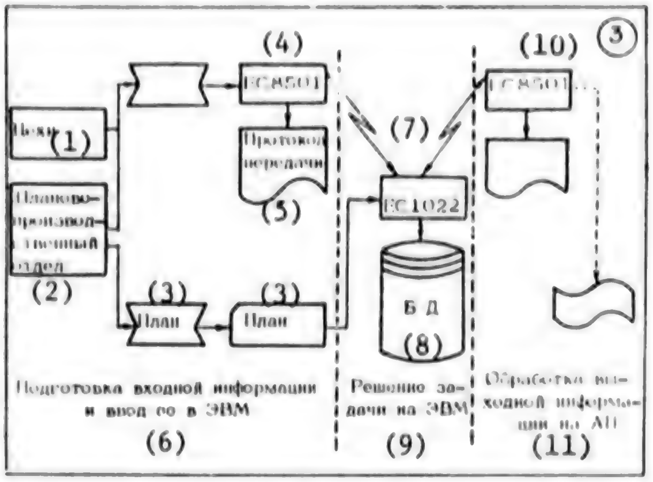
③
(4)
ЕС8501
(10)
ЕС8501
Цехи
(1)
(7)
Протокол передачи
(5)
Планово-производственный отдел
(2)
ЕС1022
(3)
План
(3)
План
Б Д
(8)
Подготовка входной информации и ввод ее в ЭВМ
(6)
Решение задачи на ЭВМ
(9)
Обработка выходной информации на АП
(11)

Fig. 3

By using these software facilities, we can use the AP-1 in the mode of operation of the AP-70 terminal.

To test the compatible operation of the AP-1 with the MPD-3 and a Unified System computer under actual conditions, we developed software for these tasks: "Operational Analysis of Course of Plan Fulfillment by Assortment," and "Compilation of Order for Dairy Products for the Finished Product Shop." These programs are operating experimentally in the teleprocessing mode as part of the ASUP [automated production control system] for the Ivanovo City Dairy Combine.

The structural-process scheme for handling the task "Compilation of Order for Dairy Products for Finished Product Shop" is shown in fig. 2. The task of "Operational Analysis of Course of Plan Fulfillment by Assortment" is shown in fig. 3.

Thus, the hardware and logic interface described has enabled operation of the YeS 8501 together with the computer and the MPD-3 multiplexer. The results of the efforts carried out allow not only expanding the capabilities of the YeSTEL complex and MPD-3 multiplexers, but also advancing specfic recommendations for use of this equipment and developing hardware requirements for terminal modernization.

Terminal compatibility with the Unified System computer MPD is among the major problems of using different-type and different-system ASU hardware.

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8545
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INSTITUTE OF CYBERNETICS WINS AWARD

Kiev PRAVDA UKRAINY in Russian 8 May 82 p 4

[Report by Ukrainian News Agency]

[Text] A significant contribution to the development of the country's economy is being made by the Institute of Cybernetics imeni V. M. Glushkov, UkSSR Academy of Sciences. The computers and systems developed here are used extensively in many sectors of the national economy. The collective at the institution maintains close ties with over 500 organizations and enterprises in the country and takes part in carrying out comprehensive programs at the union and republic level. In the past year alone, 66 developments from the institute were introduced yielding an overall economic effect of more than 50 million rubles.

For winning the All-Union Socialist Competition among scientific institutions of the USSR Academy of Sciences and union republic academies of sciences for raising efficiency and quality of scientific research efforts and successful completion of the tasks for the first year of the 11th Five-Year Plan, the collective in the Institute of Cybernetics imeni V. M. Glushkov, UkSSR Academy of Sciences, was awarded the travelling Red Banner of the USSR Academy of Sciences and the Central Committee of the trade union of workers in education, the higher school and scientific institutions.

In a ceremony on 6 May, the collective was given the award by Academician B. Ye. Paton, president of the UkSSR Academy of Sciences. He warmly congratulated the awardees and wished them further success.

Speaking on behalf of the awardees, V. S. Mikhalevich, institute director and academician of the UkSSR Academy of Sciences, expressed warm gratitude for the high evaluation of the labor by the collective and avowed that the associates at the institute will apply all their efforts, skills and experience to further develop Soviet science, to rapidly exploit its achievements in practice, and to implement the economic and social program outlined by the 26th CPSU Congress.

8545
CSO: 1863/192

MICROCOMPUTERS CONTROL PRODUCTION

Tallinn SOVETSKAYA ESTONIYA in Russian 25 May 82 p 3

[Report by ETA [Estonian News Agency]]

[Text] A system of distributed microcomputers for controlling production has been developed by scientists at the Institute of Cybernetics, Estonian SSR. Complex industrial processes in the metallurgical, chemical, paper and other sectors of industry require high precision and expeditious solutions. This is afforded by electronic computers. Practice has shown that under the conditions of major industrial complexes, where the shops, process lines and major mills are widely spread, it is more efficient to use microcomputers installed in each of the sections and united into a common system. This method of automating control is cheaper than the conventional, in which one large computer handles several different problems at once.

Problems of standardization of systems of communication between such microcomputers are also being discussed at the Tallinn seminar, which opened on 24 May, on distributed systems of computer control under the aegis of the International Federation on Automatic Control (IFAK). On the program are papers dealing with current problems in modern automatic control. Specialists from 20 countries are taking part in the three-day seminar chaired by the IFAK vice-president, B. Tamm, academician of the Estonian SSR Academy of Sciences.

8545
CSO: 1863/192

PUBLICATIONS

TABLE OF CONTENTS FROM JOURNAL 'CONTROL SYSTEMS AND MACHINES', NOVEMBER-DECEMBER 1981

Kiev UPRAVLYAYUSHCHIYE SISTEMY I MASHINY in Russian No 6, Nov-Dec 81 pp 1-2

[Text] CONTENTS Page

Shared Computer Centers and Computer Networks

Design Principles for Upper Software Levels in Computer Networks
A. I. Ilyushin, A. N. Myamlin, Vs. S. Shtarkman 3
Development of Terminal Network Access Method for Unified System OS
I. L. Dayen 12
On Automation of Modeling of Queueing System Networks with Dynamic Structure
I. V. Maksimey, Yu. A. Semishin 16
Designing Data Teleprocessing Systems in Automated Control Systems by Using the MPD-3 and AP-1; V. S. Bespalov, Ye. B. Butnikov, G. M. Strizhkov 22
Determining Reaction Time of One Class of Computer-Aided Teaching Systems
Ye. M. Sinitsa 25
An Approach to Recording Computer Technological Downtimes in the Mode of Scientific and Technical Computations; V. A. Suchilin 29

General Control Systems Design

Solving the Problem of Optimal Control of Continuous Sector Production
V. I. Dolya, P. I. Kislyakov, Ye. A. Kotovenko 31
Continuous Production Schedule Planning in Interactive Mode
V. F. Bilyuba, V. V. Kondrat'yev, S. I. Sologubov, D. G. Chulkov 38
Correlation of Industrial Plans on Computer Complexes
V. Yu. Kudrinskiy, I. P. Chernopiskiy 42

Systems Hardware and Auxiliary Equipment

Approximate Computation of Efficiency of Multibus Computer Systems
Yu. M. Sokol 45
Adaptive Control of Segment Exchange between Main and External Computer Memory
A. A. Prikhozhiy 49
YeS1010-Based Controller for Instrument Bus in IEC Standard
A. L. Kurakin, N. V. Popenko, V. N. Ryzhenkov, L. S. Sitnikov 54

Microprocessor Engineering and Application

Features of Architecture and Structure of Microprocessors and Microcomputers and Classification of Them; S. I. Yusifov 60

Questions of Implementation of BASIC Algorithmic Language in Microprocessor Systems; S. D. Pogorelyy, V. V. Sadovskiy, V. I. Teshchenko 65
Program Preparation System for Control Multimicroporcessor
R. I. Belitskiy, A. Ya. Boyko 68
System for Debugging Data Exchange Programs for Special-Purpose Computers
S. K. Goncharuk, V. I. Pustovarov, V. I. Salapatov, A. I. Flerov 70

General Control Systems Software

Interface for Graphic Representation of Programs in R-Technology
I. V. Vel'bitskiy, A. V. Moshchitskiy 73
Using Incomplete Source Information to Simplify Program
M. S. Margolin, T. P. Potapenko 78
Structural Solutions and Methods of Organizing Computing Process in Multiconsole Graphic Complex; Ye. Sh. Rayz 81
New General-Purpose Macrogenerator for Unified System DOS
I. S. Dubrovskiy 86
Real-Time DOS Simulation Model
M. G. Logunov 87
Approach to Measuring Load Factor for Real-Time Computer System in DOS ASPO [Disk Operating System Modular Software System] Environment
N. N. Merenkov, A. P. Popov 93
Text Editing in Batch and Interactive Modes
M. A. Peregudov 96
Extension of Class of Design Problems on Computer Model
A. A. Kalent'yev 101

Data Banks and Information Retrieval Systems

Some Problems of Data Bases for Integrated Management Information Systems
A. A. Morozov, G. Ye. Kuz'menko, G. A. Karpov, Yu. G. Pilipenko, V. D. Rogach 105
Data Base Layout to Minimize Media Remounting
P. Z. Bondar', G. P. Dudin, T. I. Kopysitskiy 107
Structure and Composition of Data Base for System of Computer-Aided Design and Establishing Circulation of Automated Enterprise Management System
N. T. Fisun 112
Operational Data Base Management System in Tests of Complex Engineering Objects
G. K. Matyugina, Z. A. Pavlova 114
Implementation of Static Group Locking of Data in an Information Base for a Management Information System 119

Scientific Research Automation

Recognition and Processing of Data on Topographic-Anatomic Maps in Computer-Assisted Selection of Radiotherapy Plan
V. A. Kovalevskiy, T. P. Sivachenko, V. G. Galochkin, I. N. Krupka, V. G. Sibirtsev 126

Software Packages

Software Package for Analysis and Synthesis of Uncontrolled Motion of Flying Vehicles (Principles of Design and Implementation)
V. M. Belokonov, V. D. Yelenev 129

Experience in Development and Introduction of Automated Control Systems

Design Principles for Process Control System for Large-Capacity Microbiological Production Using Microprocessors
A. A. Oprishko, A. V. Babayants, V. P. Davydov, Yu. G. Kolpikov, Ya. A. Khanukayev 133

New Hardware for Automated Control Systems

Small Multipurpose Peripheral for Microprocessor Systems
R. Ya. Chernyak, V. P. Rukhadze 137

Index to Articles Published in This Journal in 1981 139

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8545
CSO: 1863/181

MICROPROCESSORS IN CONTROL AND COMMUNICATIONS

Moscow MIKROPROTSESSORY V UPRAVLENII I SVYAZI (NOVOYE V ZHIZNI, NAUKE, TEKHNIKE: SERIYA "RADIOELEKTRONIKA I SVYAZ'") in Russian No 7, Jul 82 (signed to press 30 Jun 82) pp 2-7, 10, 16, 22-25, 28, 31-44, 60-63

[Annotation, bibliography, table of contents and excerpts from brochure "Microprocessors in Control and Communications", by Lev Abramovich Zalmanzon, professor and doctor of technical sciences, and Yevgeniy Ivanovich Pupyrev, candidate of technical sciences, Institute of Control Problems associates, reviewed by I.V. Prangishvili, Georgian SSR Academy of Sciences academician, Izdatel'stvo "Znaniye", 36,280 copies, 64 pages]

[Excerpts] Automatic control functions performed by means of microprocessors and microcomputers are described in this brochure. Concise information is given on microprocessor equipment itself. The use of microprocessors in communications is discussed.

This brochure is intended for a wide range of readers interested in questions of the application of microprocessors in modern engineering.

CONTENTS

	Page
Introduction	3
Performance of Automatic Control Functions by Means of Microprocessors and Microcomputers	6
Structure of Microprocessor Devices and Control Systems	13
Microprocessors in Communications Systems	35
Microprocessor as a Device with Program-Controlled Data Processing	44
Microprocessor Implementation of Logical Control Devices	49
Bibliography	62

Introduction

Microprocessor engineering has come a long way in the 10 years of its existence: from the creation and application of the first microprocessor integrated circuits and microcomputers designed on their basis to their mass production in all technically advanced countries of the world.

Questions relating to the application of microprocessor engineering in the area of control and communications are chiefly discussed in this brochure. In addition, brief information is presented on microprocessors now manufactured here in our country and abroad.

The first microprocessors were constructed in the USA in 1971. Comparing the status of work in this field in the USSR and USA in 1981, USSR Minister of the Electronics Industry A.I. Shokin said the following: "At the beginning of the five-year plan period the Americans wrote that we were behind them in microelectronics by approximately 8 to 10 years. And, it must be believed, they were glad of it. But by the end of the 70's their gladness had evidently diminished: Having studied some samples of our circuits in 1979, the Americans estimated the lag at 2 to 3 years. In 1981 the January issue of the American journal ELECTRONICS, and it is very authoritative in this field, already noted, and I quote: 'The technological base and skill of product engineers make it possible for the Soviet Union to manufacture integrated circuits of almost the same quality as in the USA.' And then the editorial summary states: 'The circuits obtained probably do not reflect the highest technical level of the Soviet Union in this field. The integrated circuits used in the USSR for internal needs can be technically more perfected.' We do not have any grounds for contradicting these conclusions."

With regard to what microprocessor equipment is and how it is used in control equipment, he said: "The Soviet electronics industry is now producing modern superlarge-scale and superfast integrated circuits. Hundreds of thousands of transistors combined into a complicated electronic device are contained in one such circuit the size of a graph paper square. Their speed is measured in billionths of a second. Microprocessors, representing complete microelectronic computing devices, exert great influence on the automation process. Microprocessors, and we series-produce them, make it possible to make extensive use of robots and to automate machine tools, machines, equipment and household appliances. And microcomputers created on their basis make it possible to automate complicated technological processes and planning and design and scientific research work."

Microelectronics has been advancing unusually rapidly. This is the first instance in the entire history of mankind when such rapid development of a new field of engineering has taken place. According to the data of the Ministry of Instrument Making, Automation Equipment and Control Systems, in the last five-year plan period the total output in the USSR of products using microelectronic equipment--integrated circuits, microprocessors and microcomputers--grew more than threefold and in 1980 exceeded 2 billion rubles worth. In the new five-year plan period which began in 1981 the plan is to manufacture here at home millions of microprocessors and tens of thousands of microcomputers and larger (than microcomputers) minicomputers. Complicated computer complexes whose use in the field of control is also of great practical importance are now being built on the basis of microprocessor integrated circuits.

The brochure "Microprocessors in Control and Communications" was originally written as a textbook for students in the public department of control problems at Moscow City People's University of Technical Progress and Economic Knowledge, whose operation in the Polytechnical Museum was organized by the "Znaniye" [Knowledge] Society and the Institute of Control Problems. In general special knowledge is not required in order to read this brochure.

In terms of the degree of integration of elements the distinction is made between small-scale integrated circuits (MIS's), medium-scale (SIS's), large-scale (BIS's) and superlarge-scale (SBIS's). A large-scale integrated circuit contains from 1000 to 10,000 functional elements (a superlarge-scale integrated circuit more than 10,000).

Let us give as an example a description of the controller from the article by Yu.M. Yeremeyev et al. (cf. bibliography). In this controller, designed on the basis of the domestic "Elektronika S5-11" microcomputer, the possibility is provided of implementing six different control principles, the signal conversion error is less than 0.6 percent, the time for a single cycle is 0.05 s, and tuning factors can be varied over a wide range (gain from 1 to 127, integration constant from 1 to 127 s, differentiation constant from 0.01 to 0.99 s and quantization period from 0.01 to 0.32 s).

An idea of the degree of complexity of a microprocessor is given in fig 1b, in which is presented a more detailed diagram of the domestic K580IK80 microprocessor (an analogue of the 8080 microprocessor).

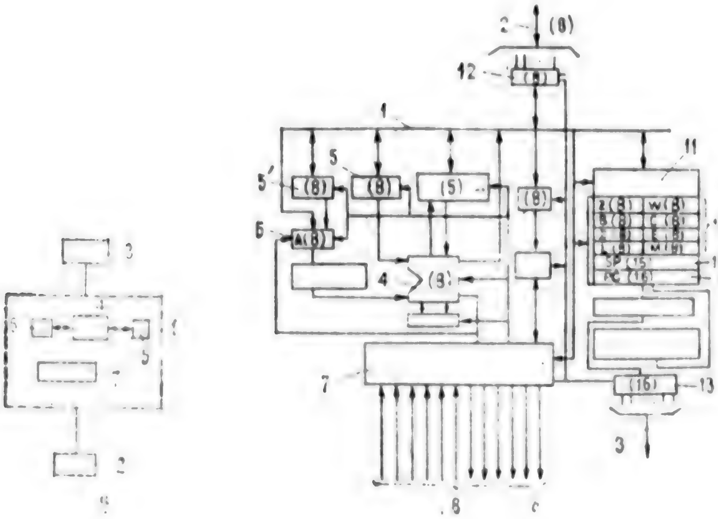


Рис. 1.

Figure 1.

A diagram of the "Elektronika S5-12" microcomputer--one of the "Elektronika S5" microcomputer series designed on the basis of the p-MOS technology--is presented in fig 2b. The main component of this microcomputer is the 16-bit microprocessor, 1, described above. The microcomputer's internal memory includes four ROM's, 2, with a total capacity of 2048 16-bit words and four RAM's, 3, with static storage of data and a total capacity of 128 16-bit words. The microcomputer is linked with peripheral devices by means of four input and output control large-scale integrated circuits, 4, contained in it (a total of 32 channels for input and output of digital signals).

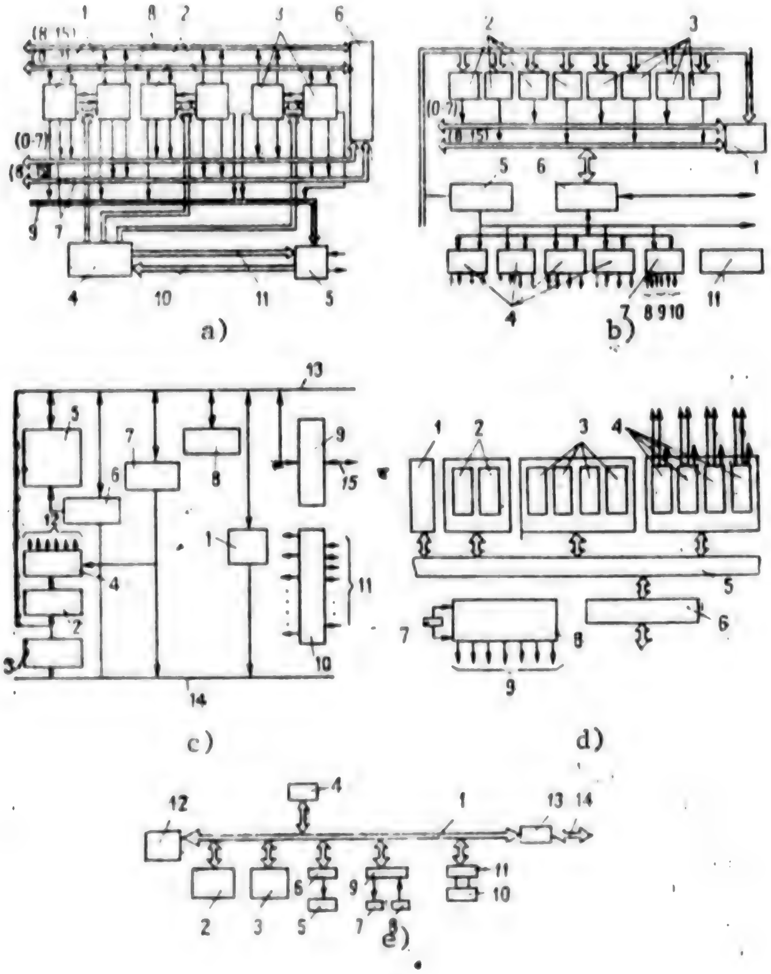


Figure 2.

The next representative of the "Elektronika S5" series is the "Elektronika S5-21" single-board microcomputer and the microprocessor functional modules (MFM's) developed along with it and constructed with large-scale integrated circuits implemented by the n-MOS technology. The latter's use made it possible to increase the number of transistors on a chip to 8000 with an irregular large-scale integrated circuit structure and to 20,000 with a regular, and also to increase speed of response. A single-chip 16-bit microprocessor, a 16K-bit-capacity ROM and a 1K-bit-capacity RAM and a multifunctional data input/output device are the basic large-scale integrated circuits for this part of the "Elektronika S5" series.

In the microcomputer there is a frequency divider, 8, connected to a frequency oscillator, 7, and from whose output channels, 9, signals with various fixed frequencies (1200, 600, 120, 15, 7.5 and 1 kHz and 100 and 1 Hz) are picked up. Obtaining a set of stable frequency signals is useful for a number of applications. Among the microprocessor functional modules designed for expanding the operating capabilities of systems with microcomputers are RAM and ROM modules, modules for interfacing with peripheral devices, etc.

Of other series of microcomputers developed in the USSR let us point to the "Elektronika NTs" series. A set of different large-scale integrated circuits is used for constructing this series of microcomputers and control microprocessor devices. Various microprocessor systems are designed with these large-scale integrated circuits. One of their main purposes is to control various entities. Their use as built-in functional components of control systems has been provided for. Microcomputers of this series, which can be easily joined together, are adapted also for use in multiprocessor computing systems serving the purpose of processing large data arrays. The same RAM's and ROM's are used for various models of microcomputers of this series.

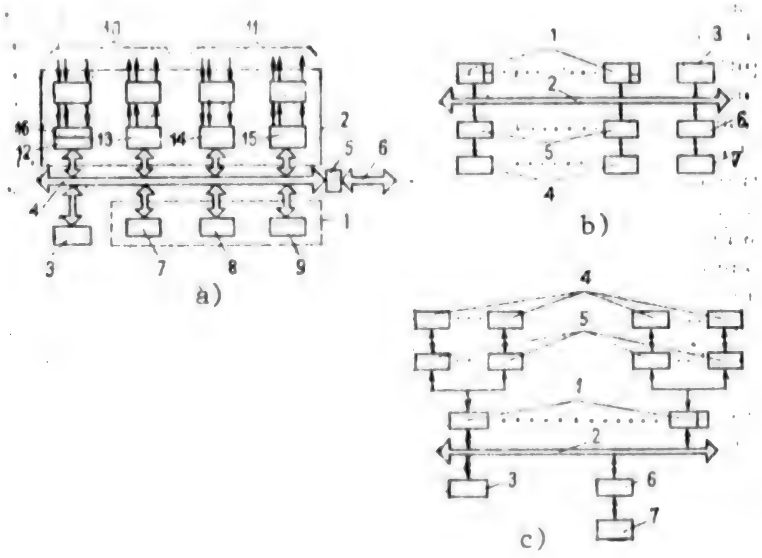
"Elektronika NTs-03" microcomputers, in particular the "Elektronika NTs-03T" microcomputer, are typical representatives of this series. This group of microcomputers is constructed with large-scale integrated circuits implemented by utilizing the CMOS technology. The microprocessor here is a single-chip 16-bit one.

Two varieties of "Elektronika NTs-03" microcomputers are manufactured in completed form. One of them is the "Elektronika NTs-03T" mentioned, whose general structural diagram is given in fig 2e. The distinctive feature of this microcomputer is the presence in it of a unified internal trunk, 1, to which are connnected up to 16 processors, 2, a RAM, 3, control console, 4, typewriter, 5 (connected via a controller, 6), punch, 7, and a punched tape photoelectric reader, 8 (connected via controller 9). Provision has also been made for connection to the internal trunk, 1, of various devices by means of a programmable interface, 10, with 32 input and 32 output channels connected to the trunk via controller 11. The trunk's control unit, 12, is also shown in this figure. Trunk 1 is connected to external trunk 14 via board 13 which serves the purpose of matching signal levels. Another distinctive feature of this microcomputer is the asynchronous principle of its functioning, because of whose use it is possible for the microcomputer to operate together with devices having various data interchange speeds. The reader will find a more detailed description of microcomputers of the "Elektronika NTs" series in the book "Mikroprotsessornyye BIS i mikro-EVM" [Microprocessor Large-Scale Integrated Circuits and Microcomputers] edited by A.A. Vasenkov and listed in the bibliography.

Other microprocessors and microcomputers (the "Elektronika-60", "Elektronika K1-10", "SM-1800", etc.) have been developed in the USSR. Much attention is now being paid to improving single-chip microprocessors.

Cross facilities for automation of programming designed for using general-purpose BESM-6, YeS [Unified Series] and M-220 computers have been developed for domestic microcomputers of the "Elektronika S5" series. The BESM-6 computer is also used for cross programming in development of microcomputers of the "Elektronika NTs" series. There are also resident (i.e., found in the microcomputer itself) facilities for automation of programming.

Let us go to the third type of control system which we have singled out. There is only a single processor in the system shown in fig 4a. When processing more information than in the relatively simple cases discussed, it is advisable to use multiprocessor control systems, or, as they are otherwise called, mutliprocessor systems. The need to use multiprocessor systems arises where it is necessary to process large arrays of data which can be multiprocessed. By connecting a number of processors for running various parts of a program, it is possible to speed data processing to such an extent that it becomes possible to control in real time even fairly complicated entities. Much attention is being paid now to the question of the structural organization of multiprocessor systems. Some of the circuits for designing them described in the literature are discussed below.



a)

b)

c)

Figure 4.

One variant of a mutiprocessor control structure is illustrated in fig 4b (it is possible to become acquainted in greater detail with the circuits presented in this figure through the article by L.L. Agronin et al.; cf. bibliography). Here there are several groups of central processors, 1, with their own RAM's and ROM's, connected via a system interface, 2, with the RAM for the entire system, 3, and with a series of input/output devices, 4 (the latter are connected via interface modules, 5). When necessary, by means of system interface 2 the devices indicated above are connected via interface module 6 with a higher-level computer, 7. This system can, as compared with a single-processor system, speed up to a great extent the processing of data upon condition that the rate of transfer of data between input/output devices and other components of the system is not restricted by the system interface.

More efficient in this respect is the system shown in fig 4c. It is characterized by the fact that there are internal interfaces and each processor serves an individual group of input/output devices independently of the others. The designations in fig 4c are the same as in fig 4b. Here the multisystem organization of the control process is essentially already illustrated, since each central processor with its own group of interface modules and input/output devices forms a system which independently controls a given group of devices, and only to the extent to which it is necessary linked via the system interface with other similar groups, with the system's RAM and, possibly, with a higher-level computer.

It is advisable to use these circuits for controlling a number of input/output devices in cases when it is not necessary to process very large data arrays. Otherwise it is necessary to add to the microprocessor system special high-throughput control computer complexes. We will discuss systems of this kind separately. Let us place them under the heading of the fourth type of the number mentioned by us.

The use in a microprocessor system of a high-throughput computer complex proves to be necessary when, for example, in controlling a complex system it is necessary to form a model of it in real time (let us recall what was said at the beginning of this brochure regarding new methods of control whose implementation became available with the creation of microprocessor equipment). This became possible because of the fact that many operations performed in controlling complex systems are easily multiprocessed and consequently can be performed simultaneously. They include, for example, a fast Fourier transform (BPF), digital filtering of signals, computation of correlation functions and various operations with vectors and matrixes.

High-throughput control computer complexes based on microprocessor equipment--the PS-2000 and PS-3000 computer complexes--have been developed in the USSR. Computer complexes of this kind, designed on the basis of computers with a uniform reorganizable structure, are used in geophysical expedition systems, where there use made it possible to improve substantially the processing of seismic prospecting data in prospecting for oil and gas deposits and deposits of minerals, and in performing work associated with forecasting earthquakes. These computer complexes can be used in various microprocessor control systems which process large arrays of data.

Let us indicate the key characteristics of the PS-2000 control computer complex. It contains a group of processor elements operating with unified control and interconnected in a unified manner. The number of processor elements is chosen to equal 8, 16, 32 or 64. Each processor element is furnished with its own RAM with a capacity of 12K bytes or 48K bytes. With the minimum 8-processor and maximum 64-processor configurations the throughput of this multiprocessor computer complex equals, respectively, 25 million or 200 million short operations per second. The speed of performance of various operations in a single processor element is from 0.3 to 2.2 μs. With 64-processor elements the time for execution of a fast Fourier transform for 1024 complex numbers with base 2 equals a total of 1 ms.

Microprocessors in Communications Systems

Wire and radio communications come under the heading of basic areas of application of microprocessor equipment. Because of the use of microprocessors and microcomputers for digital processing of signals it has proved possible to increase the carrying capacity of channels, to improve noise immunity and to expand the functions performed by communications equipment. Work on the creation and use of microprocessor equipment of this kind is being done extensively in the USSR and abroad.

One typical application of domestic microcomputers of the "Elektronika S5" series is subscriber's stations of telegraph and telephone communications systems. The number of microprocessor modules for constructing systems with expanded functional capabilities includes the "Elektronika S5-124" special module for interfacing with a telegraph set (TA). When using microcomputers at subscriber's stations it is possible to perform successfully such functions as data interchange with punched tape input/output units and a unit for inputing messages for printout; preparation and editing of data when using an electric typewriter; and signal conversion.

How noise immunity is improved when microcomputers are used can be judged from data on communications systems constructed in the USSR. For example, unreliability of signal transmission when working with microcomputers equals not greater than $2 \cdot 10^{-6}$ for a communications channel with error probability of 10^{-3} per character. The effectiveness of the use of microprocessor equipment in telephone communications systems can be judged on the basis of the following. According to the estimates of specialists, in creation of automatic telephone exchanges the use of microcomputers makes it possible to reduce the cost of communications facilities 1.5-fold, to reduce the consumption of electric power approximately 3-fold and to increase considerably the reliability and carrying capacity of telephone lines.

The experience gained by foreign firms which produce microprocessors and microcomputers, as well as by specialized firms involved in manufacturing communications equipment, is indicative. The more efficient use of communications channels is achieved by various methods. For example, on the basis of the 8085A microprocessor Intel has constructed a system making it possible in transmitting a conversation through a telephone channel to use for the purpose of transmitting other conversations the pauses existing in this conversation. These pauses occur since usually a telephone channel is not occupied the entire time when a conversation is transmitted--only one half the time or even less on average. On the basis of microprocessors and individual large-scale integrated circuits equipment has been developed which makes it possible for a party to use the automatic dialing system, using pushbutton dials, and to use equipment making it possible to store in the computer memory (to access it when necessary) the numbers of telephones to which calls have been made.

Typical of new developments is the diversity of forms of signal processing. Serial transmission of signals has been combined with the widely used multiprocessing of them. Ever greater importance has been taken on by communications systems designed for data interchange between a human being and a computer and for transmission of large arrays of data from some computers to others (so-called data transmission systems). Their role is growing all the time, since the amount of information used is increasing substantially every year with the development of science and engineering. Here in our country this problem is being solved by creation of the OGAS--the All-State Automated System of Data Acquisition and Processing for Accounting, Planning and Control of the National Economy.

Microprocessors and microcomputers are being used in creation of various kinds of communications system equipment, such as encoders, decoders, modulators, demodulators, etc. What are these devices? What functions do they perform? In order to answer these questions let us talk briefly about the general structure of digital communications systems. Then we will give examples of the use of microprocessors and microcomputers in foreign wire communications equipment and we will discuss one typical example worked out here at home of the improvement of a radio communications system on the basis of using microcomputers.

Structure of Digital Communications Systems

The following method of processing and transmitting signals in digital communications systems is the one generally used. The source information, continuous or discrete, is represented in digital form convenient for transmission. Signals are transmitted by the frequency method--frequency-shift-keyed signals are used. Received signals are processed in order to recover the source information. Here the total system for transmission of signals in a single direction is as shown in fig 5a, where 1 is the transmitter, 2 the receiver, 3 the communications channel and 4 is the return channel through which signals regarding errors detected by the receiver arrive at the transmitter (with the arrival of this information signals previously received with an error are retransmitted). If the source information is continuous, then prior to the arrival of signals at the transmitter their analog-digital conversion is performed by means of an analog-digital converter (ADC). Signals are first time quantized: Samples are taken of the transmitted quantity at discrete moments of time. By means of a special device--an encoder--these samples are coded in terms of level in order to obtain a digital representation of them permitting their transmission through a communications line with maximum speed and minimum distortion. High-frequency electrical oscillations are constantly transmitted through the communications channel. In the receiver there are a demodulator and decoder which perform conversions the opposite of those which are performed by the transmitter's modulator and encoder, respectively. By means of a digital-analog converter (DAC) the digital signals received are converted into continuous. The transmission of discrete signals is accomplished in the same way. Only the need to use an ADC and DAC disappears. If the source discrete information is not represented in digital form, then in order to reduce it to it, as well as for the purpose of performing reverse conversion, a discrete-digital converter and digital-discrete converter, respectively, are used which perform simpler functions than an ADC and DAC. Since even with one-way transmission according to fig 5a it is necessary to send signals in both directions (the main signal and that carrying information regarding errors), the need arises to use in the transmitter and receiver combined modulator-demodulators and encoder-decoders. The first of these are called modems and the second codecs.

In the transmitter, in addition to a modem and codec, there are usually units which serve the purpose of interfacing with the information source, of protecting from errors and of coordinating the operation of the transmitter's elements and of controlling the operation of the system. Similar units are present also in the receiver, only here functions of interfacing with the information receiver are performed. Interface units contain memory registers which store data to be retransmitted in the case of detection of errors. Protection units are used to improve the noise immunity of communications systems. This is achieved by introducing additional signals which serve the purpose of detecting and eliminating distortion in transmission of information. In digital communications systems other equipment is also used, also constructed on the basis of using microprocessors and microcomputers. It includes equipment for synchronizing transmission beats and cycles in multichannel digital radio communications systems, equipment for automatically tuning the frequency and phase of oscillations in digital signal demodulators, and various pieces of equipment for time-division multiplexing of channels. The latter is performed in order to unite ("compress") an entire series of sequences of digital signals to be transmitted into a unified combined sequence in order to again separate the original sequences at the end of the transmission process.

In this manner, as well as by using special methods of modulating and encoding signals, an increase in the carrying capacity of communications channels is achieved.

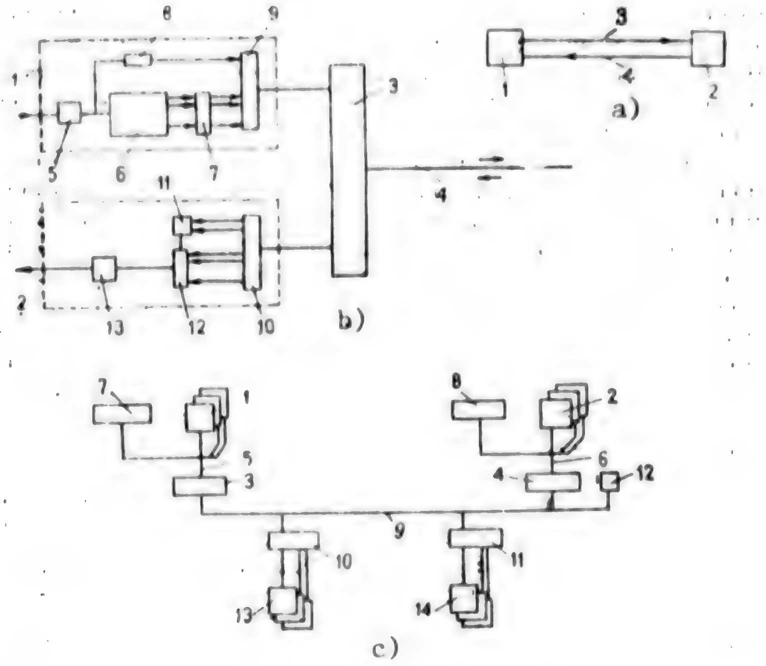


Figure 5.

The coding of signals is performed by various methods in different cases. So-called pulse-code modulation (PCM) and delta modulation are employed.* With PCM each sample is encoded in terms of level independently. With delta modulation the value of the encoded quantity is compared at each of the discrete moments of time sampled with its value at the preceding moment of time and a determination is made of the value of the difference of these quantities. The encoding of signals by one method and the other is performed so that their automatic decoding is possible at the other end of the communications line. Tuning of equipment whereby encoding intervals are selected in the most advantageous manner in each case is optimum. Special methods of data processing are employed whereby samples of the converted quantity are regarded as random quantities and the transmission control process is carried out in order to make possible maximum speed of signal conversion and transmission with minimum errors. In transmission of voice signals special methods of digitally encoding them are employed whereby an analysis is first made in the transmitter of signals to be transmitted and then they are restored in the receiver. Extensive opportunities for performing all of these functions have appeared because of the use of microprocessors and microcomputers in communications systems.

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*These names are not totally successful. Actually, the word "modulation" is used here not in the same sense as indicated above. In this case it is a question of encoding and not of modulating signals. In order to avoid misunderstandings resulting from the incorrect names "pulse-code modulation" and "delta modulation" (which, however, are generally accepted), sometimes, as we did at first, the expression "manipulated signals" is used instead of speaking of modulation of signals when it is actually being performed.

Examples of Use of Microprocessors and Microcomputers for Processing Signals in Digital Wire Communications Systems

Microprocessors are used in creation of so-called digital voice terminal units in which first an analysis is made of human speech in its transmission through a communications channel and this speech is synthesized from signals received at the end of the transmission line. A system for digital microprocessor processing of voice signals in real time designed on the basis of an Intel 3000 microprocessor contains a processor connected to an ADC when analyzing speech and to a DAC when synthesizing it. The processor is connected to a microinstruction storage and a RAM, used in the process of operation of the microprocessor system. Various microprocessor circuits are employed for digital encoding of speech. One of them, accomplishing so-called linear forecasting encoding, is shown in fig 5b. The operation of this encoding system is based on the fact that a forecast is made of digital signals taking into account signal samples preceding in terms of time. Individual correlation functions are taken into account in calculating forecasting factors. In addition, by means of calculations performed by the microprocessor unit a determination is made of parameters characterizing the pitch of a tone and the sonority of the speech. The original speech information is restored from these data in decoding after signal transmission. A microprocessor system for digital processing of human speech (fig 5b) has a signal encoding unit, 1, and a unit for decoding them, 2. Both units are connected via a modem, 3, to the communications line, 4. Unit 1 contains an ADC, 5, circuits for computing correlation functions, 6, and forecasting factors, 7, a tone and sonority detector, 8, and an encoder, 9. In unit 2 there are a decoder, 10, a circuit for reacting to the pitch and sonority of speech signals, 11, a voice synthesizer, 12, and a DAC, 13.

In some digital voice terminals which have been developed, e.g., in the one made by Fairchild, designed with microprocessor modules, encoding of voice signals is performed by the method of adaptive differential PCM, with which a speed of transmission through a communications line of up to 30K bits of information per second is made possible. Even higher signal transmission speed is achieved by means of special code converters. One such microprocessor signal conversion and transmission system was designed for working together with the IBM NOVA-3 minicomputer.

A number of microprocessor systems for noise-immune encoding have been developed. The program for one of these systems, implemented on the basis of an Intel microprocessor, provides for execution of the so-called Witherby decoding algorithm. It is based on using a code with correction of error bursts: Code combinations to be decoded in the receiver are compared with reference combinations which are stored in the memory of the decoder and from computed correlation functions a determination is made of which of them a given code combination corresponds to. In other microprocessor systems operating with noise-immune encoding a serial decoding algorithm is employed whereby each information character is decoded separately on the basis of comparing a sequence of signals with a reference sequence, which can also be accomplished by determining the correlations between them. A feature of this algorithm consists in the fact that the decoding time changes automatically depending on the number of errors to be corrected in transmission of information.

Research carried out has shown that by means of microcomputers it is possible to transmit signals with effective correction of errors and distortion. In the literature on microprocessor communications systems the data of experiments are given in the course of which, with probability of error in input information of 10^{-2} , probability of error in the system's output of $7.5 \cdot 10^{-5}$ was gotten when using the Witherby decoding algorithm and of $9 \cdot 10^{-5}$ with serial decoding.

Microprocessors are used also in constructing programmable digital modems. Digital modems of two types have been developed: Under the heading of the first come relatively inexpensive ones having relatively slow speed of response and designed for mass use in transmission of signals through standard telephone channels, and to the second high-throughput modems designed for modulation and demodulation in processing large amounts of information. An example of digital modems of the first type is modems for processing phase-shift-keyed signals designed on the basis of the Motorola 6800 microprocessor. In their operation, as in other digital modems, a great number of samples of signals are stored for whose transmission the components of harmonic oscillations forming the carrier modulation system are used.

For performing the functions of programmable modems in transmission in real time of much digital information, special-purpose microprocessor systems have been developed by means of which more ideal algorithms are implemented for modulation and demodulation of signals, such as, for example, the adaptive compensating algorithm. In these special-purpose digital modems in addition to the processor there are a number of other functional units, including a ROM which stores the initial factors for the adaptive signal converter (filter) and other unchanging data, a RAM for storing factors used in instantaneous transformations performed by the adaptive filter and for storing input data, a processor-synchronized instruction counter and memory addressing units.

Use of Microcomputers in Radio Communications Systems

In radio communications systems microprocessor units perform functions similar to those discussed above, and a number of other functions. Typical, for example, is a multiprocessor automatic control system which must establish communications on line and then maintain them reliably with the operation in addition to the assigned transmitter and assigned receiver of a number of other radio electronic communications facilities (RES's) also, and with the presence of lines used by them collectively. The main thing here is to find in the shortest possible time the transmission frequency optimum for a given channel. Only the use of the authorized frequency band is permissible; frequencies must be provided for service broadcasts, etc. The automatic control system must make possible operation of the channel formed and a check must be made of the correctness of its functioning. The circuit of a microprocessor automatic control system designed for performing these functions is given in fig 5c (developed by M.Ye. Vishnevetskiy, A.D. Kaluzhskiy, V.I. Kontorovich and Yu.K. Lyudayev). The following designations are used in fig 5c: 1--group of RES's of the system's transmitting section;

2--group of RES's of the system's receiving section; 3 and 4--microcomputers which check and control groups 1 and 2, respectively; 5 and 6--collective-use lines intermediate between 1 and 3 and between 2 and 4 in one and the other group of RES's; 7 and 8--internal testing and control equipment in groups 1 and 2. Control of the operation of microcomputers 3 and 4 is performed through signals transmitted through main collective-use line 9 from testing and control units 10 and 11 and from frequency discrimination units 12, also designed on the basis of microcomputers. Units and 10 and 11 are directly connected to the control panels of operators 13 and 14 (instructions are transmitted by means of telephones, teleprinters and other primary control facilities). The developers of this system have recommended that domestic K580 IK 80 microprocessors be used in designing the system. They noted that for the number of RES's serving the purpose of forming 50 communications channels, for the purpose of performing the required functions, in the above-described system it is sufficient to use five microcomputers operating at a speed of $2 \cdot 10^5$ operations per second with a total memory capacity of 10K bytes for each microcomputer. With this the time for forming a channel is reduced to a few seconds from 3 to 5 min in the radio communications systems now used which operate without microprocessor processing of signals.

General information on microprocessor engineering equipment and on its use in the field of control and communications was presented above. In the next two sections of this brochure a more detailed discussion is presented of questions relating to the operation of microprocessors as devices with program-controlled data processing and to the performance of logic functions by them.

In addition to the performance of logic functions by general-purpose microprocessors, microprocessor equipment is also used which is specially oriented toward implementation of logic functions and complicated logical control algorithms. They are designed on the basis of standard microprocessors or by using special-purpose microprocessors.

Under the first heading comes, for example, the program logic control unit of the LIUS-2 hardware complex developed in the USSR. It is constructed with series K589 word-length-expandable microprocessors.

In equipment of the second type, to the common trunk with a basic standard microprocessor such as, for example, a K580 IK 80, is connected an additional "logical" processor designed in a special manner. Here computation of logic functions is performed considerably more quickly than would be possible when using only the single main processor. In these systems the main processor carries out general control of the system and implementation of logic functions is entrusted to the additional processor.

Of foreign systems of the latter type let us point out as an example the PJ 40 microcomputer (FRG). It contains a Zilog 80 main microprocessor, a logical processor, a memory for storing the operating system and working storages. The logical processor contains an operating unit which performs computations and a working storage with a 1K-byte capacity. The logical processor's storage is divided into four parts. One part stores the values of input signals, another the values of output signals, a third part of the memory stores information on the previous state of the controlled system, and the last part of the memory stores information on the current state of the system.

In addition to hardware enabling high speed of response in computation of values of logic functions, various kinds of software are also provided in this microcomputer. This includes the general operating system and a special operating system for implementing logical control algorithms. The latter has a special set of control instructions and facilities for describing various elements of industrial automation equipment, including logic elements, flip-flop relays and the like.

Extensive opportunities for increasing the throughput of microprocessors and microcomputers implementing logic functions, as well as other control functions, are evidenced in multiprocessing of problem-solving algorithms.

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